Indira Gandhi National
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BPHCT-143
DIGITAL AND ANALOG CIRCUITS AND INSTRUMENTATION

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Volume – II Blocks 3 & 4

Volume II

Indira Gandhi National
Open University
School of Sciences

BPHET-143
DIGITAL AND ANALOG CIRCUITS AND INSTRUMENTATION

Block

4

OPERATIOINAL AMPLIFIER AND INSTRUMENTATION

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CONTENTS

BLOCK 4 : OPERATIONAL AMPLIFIER AND INSTRUMENTATION

In this course, so far you studied the analog and digital circuits built using discrete semiconductor components. The amplifiers and oscillators use transistor as their basic component. Such circuits are useful to a limited extent, since the discrete components make them very bulky. The advances in semiconductor technology reduced the component size and it was possible to build several circuits on a small silicon chip. These are called Integrated Circuits (ICs). We get the ICs for various applications like gates in digital circuits, amplifiers, power supplies etc.

Most widely used analog IC is the **operational amplifier** or **"op-amp"** in short. This is a very versatile amplifier circuit with two inputs, which can be used to perform mathematical operations like addition, subtraction, multiplication, division, differentiation, integration of input signals.

Op-amp has very special characteristics like very high gain, high input impedance and low output impedance. It has good ability to reject the noise riding on the input signal lines due to its differential mode of operation.

In **Unit 13**, you will learn about the basics of op-amp and its characteristics. Some important applications of op-amp are discussed in **Unit 14**. You have used the cathode ray oscilloscope (CRO) in the laboratory course of first semester to obtain the Lissajous Figures. In **Unit 15** we will describe the features of CRO in details.

In the second block of this course you learnt that the digital circuits work on only two voltage levels and a train of high-low voltages make a digital signal. Generation of square waves or pulses is very useful in electronics. Sometimes the start of the pulse can also be varied depending on some external signals. This type of pulsed signals can be generated using multivibrator circuits. The most common IC used as multivibrator is IC555 timer. You will learn about its working and design of the astable and monostable multivibrators in **Unit 16**.

We wish you all the best for your studies.

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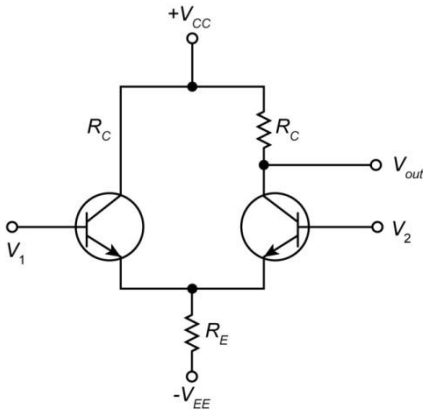


Differential amplifier forms the first stage of operational amplifier. It provides two inputs – inverting and non-inverting – as you will learn in this unit.

UNIT 13

OPERATIONAL AMPLIFIER

Structure

STUDY GUIDE

In the last block you learnt about the analog circuits used in electronic systems. In this unit you will learn about a special kind of amplifier with two inputs used for performing mathematical operations like addition, subtraction, multiplication of analog signals. This is operational amplifier. To understand this unit well, you should revise Unit 10 on Amplifiers from the last block. You should also revise the concepts of input-output impedances, gain etc. to appreciate the discussions here.

You should solve the SAQs and Terminal Questions on your own for better understanding of the content.

"Op amp offers all the advantages of monolithic integrated circuits: small size, high reliability and reduced cost."

Jacob Millman

13.1 INTRODUCTION

Operational Amplifier (Op Amp) was first designed in 1948 based upon a single vacuum tube. The primary use of early op amps was in analog computers. The op amps derived their first name "*operational*" basically because at that time they were used in mathematical operations such as addition, subtraction, multiplication, division and solving differential equations.

The limited accuracy of analog computers up to three significant figures had limited their use. They were later replaced by digital computers which were faster, more accurate and versatile.

With the advancement of integrated circuit (IC) technology, several types of IC based op amps were produced in mid-sixties which were available in the market. These op amps required much lower power as compared to the discrete components based amplifiers. They were cheaper and needed much less space. With such op amps commercially available, the task of designing circuits became very easy. With one or two op amps and a few resistors or some other components, very good quality amplifiers, signal generators, modulators, etc. could be made.

The sophistication in the recent times in the IC technology enabled the manufacturers to produce special purpose op amps. The dual and quad op amp packages have two and four op amps respectively on a single chip. They are commercially available and are quite cheap.

As a user of an op amp it is sufficient to know its basic building blocks on a schematic diagram. It is not required to know the detailed component level circuit of the operational amplifier which is grown on a single IC chip. What we need is the performance characteristics of the op amp available in the data sheet supplied by the manufacturer. With such characteristics known, we can use the op amp in various applications.

In Sec. 13.2 you will learn the basic blocks of op amp. In Sec. 13.3 we will describe the technical details of commercially available op amp ICs.

In Sec. 13.4 we will discuss in details the important characteristics of op amp that affect its performance. We will also compare the characteristic parameters of commonly used op amp IC 741C with that of an ideal op amp.

In the next unit you will learn about some important applications of op amp.

Expected Learning Outcomes

After studying this unit, you should be able to:

- draw the block diagram of an op amp;
- describe the concept of inverting and non-inverting inputs of an op amp;
- draw a schematic symbol for an op amp;
- distinguish between the two types of packages of op amp IC;
- draw the pin-out diagram for op amp IC 741C;

- ❖ interpret the number code printed on the IC;
- ❖ explain the power supply requirements for op amps;
- ❖ state precautions which have to be taken while working with op amps;
- ❖ establish input-output voltage relationship for op amps;
- ❖ draw the ideal voltage transfer curve for an op amp;
- ❖ define input offset voltage, output offset voltage, input impedance, output resistance, common mode rejection ratio, maximum output current, power consumption, slew rate and gain bandwidth product; and
- ❖ compare the characteristics of ideal op amp and of IC 741C.

13.2 BUILDING BLOCKS OF AN OPERATIONAL AMPLIFIER

Operational amplifiers are very special type of amplifiers which are designed by cascading multiple stages of different types of amplifiers. You have learnt most of these types in Unit 10 of this course. Fig. 13.1 shows the basic building blocks of a typical operational amplifier. It comprises many stages.

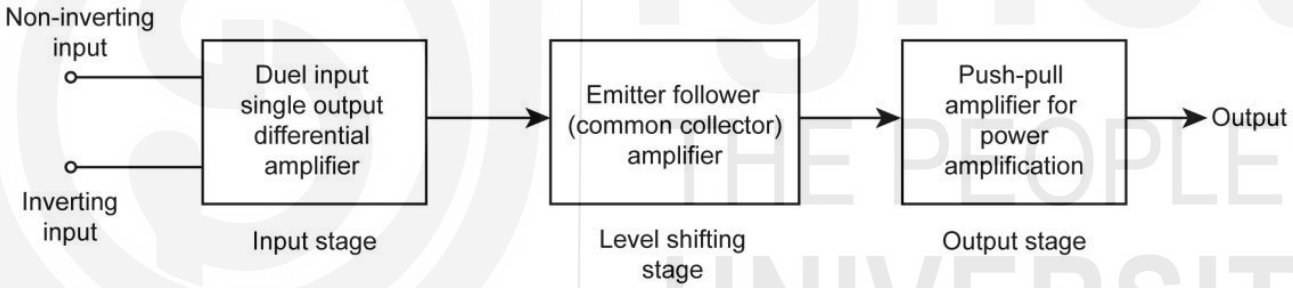


Fig. 13.1: **Block diagram of an op amp.**

In this diagram the first stage is a special type of amplifier which has two inputs and its output is generated depending upon the difference between these two inputs. Such amplifiers are called **differential amplifiers.**

The second stage, called level shifter is required because on the integrated circuit chips, it is difficult to build capacitors. Hence, the capacitive (ac) coupling between the two stages of amplifier is not possible, and the dc level riding on the amplified signal from the differential amplifier output has to be removed by a special level shifter circuit, which is typically a common collector amplifier. Usually the output of an op amp is used to drive the loads, which may require high currents. Hence, the last stage of op amp is a power boosting stage in the form of a push-pull amplifier.

The differential amplifier is a circuit made of two matched transistors (i.e. their type, gain, impedances, V_{BE} value etc. are equal). The collector and emitter of these two transistors are joined together to the supply voltages V_{CC} and $-V_{EE}$ through equal resistances R_C and R_E respectively, as shown in Fig. 13.2a.

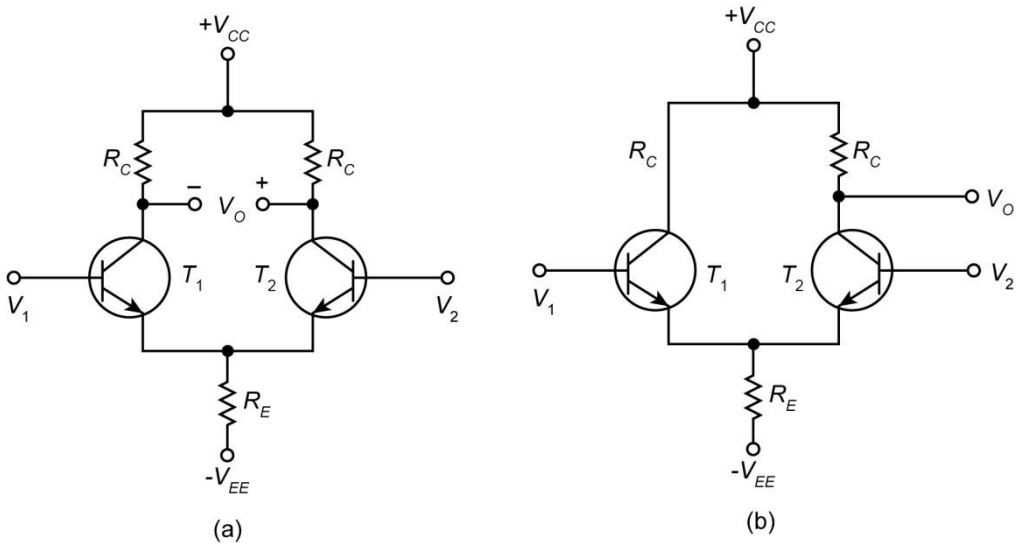


Fig. 13.2: **Differential amplifier: a) basic configuration; b) double ended input and single ended output.**

Due to matching transistor parameters, if the input voltages V_1 and V_2 are equal, equal currents flow through both of them and the output V_0 is zero. But if V_1 is more positive than V_2, then the polarity of V_0 is as shown in the figure. It is clear that the output signal at the collector of T_2 is in the same phase as V_1 (input of T_1). Hence the input of T_1 is called the **non-inverting input**. In contrast, the output is 180° out of phase with respect to the input of T_2. Hence, it is called the **inverting input**.

At times, the op amp output is taken from the collector of T_2 and measured with respect to ground potential as shown in Fig. 13.2b. This configuration with double ended input and single ended output is most commonly used in practice. In this unit will consider this configuration of op amp only.

After getting familiar with the inputs and output of operational amplifier, in the next section we will look at some technical details of op amp ICs.

13.3 TECHNICAL DETAILS OF OP AMP

Before learning the usage of op amp, you should get familiar with some general technical details of op amp ICs and associated requirements like power supplies etc.

13.3.1 Symbol

The symbol used for op amp is shown in Fig. 13.3. It is a triangle pointing to the signal flow. This symbol also shows the terminal (or pin) numbers for a general purpose and very popular op amp integrated circuit – IC 741C. All op amps have at least five terminals – two for inputs, two for power supply and one for the output. General purpose 741C has some other terminals as well.

The op amp has two input terminals. Pin 2 is the inverting input. When the input is given to it, the output at pin 6 is available with 180 degree phase change. Pin 3 is the non-inverting input. The input given to this pin is available at pin 6 without phase change. The inverting input (pin 2) is often shown with

a (–) sign and non-inverting input (pin 3) with a (+) sign. These two terminals are known as **differential input terminals**. The output voltage depends upon the difference in voltages between them.

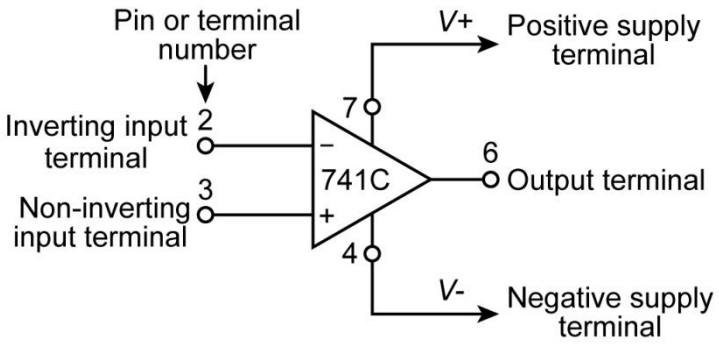


Fig. 13.3: **Symbol for an op amp.**

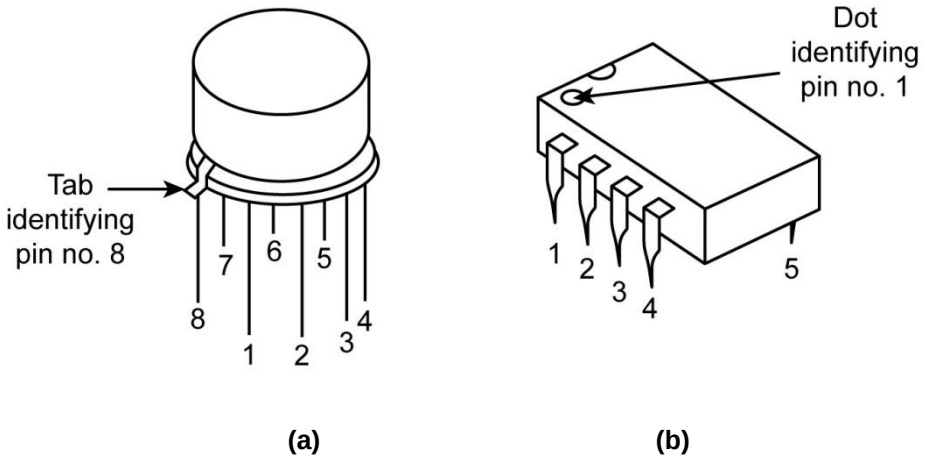
The op amp requires a dual power supply; means a positive as well as negative voltage supplies are used. Negative voltage terminal of the dual power supply is connected to pin 4 and positive voltage terminal is connected to pin 7. Note that if the polarities of the voltages applied to pins 4 and 7 are reversed, the op amp shall be damaged and cannot be used any more.

SAQ 1 – **Pins of op amp**

What are the numbers of input and output pins of IC 741C?

13.3.2 IC Packages

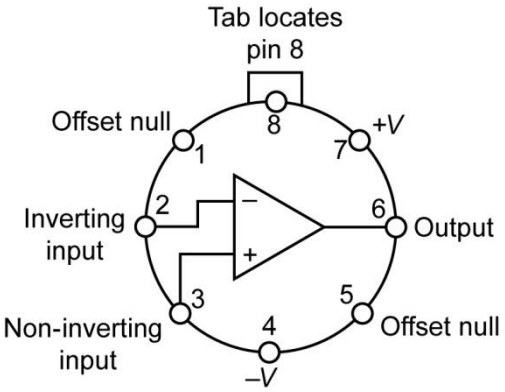
The op amp which is fabricated on a silicon chip is housed in a suitable package. Op amp 741C is available in two most popular packages (a) metal can and (b) dual in-line packages (DIP). These packages are shown in Fig. 13.4a and b respectively. This IC has eight pins (or terminals) to connect it in the circuit. The metal can IC is round in shape and pin number 8 is indicated by a tab protruding out from the metal package. The DIP packages are in plastic casing. Pin number 1 is indicated by circle or dot engraved on the top of the IC package.



(a) **(b)**

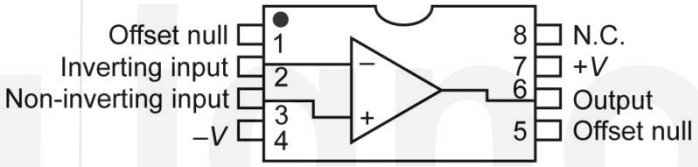
Fig. 13.4: **Op amp packages: a) metal can; b) 8-pin DIP package.**

The combination of the op amp symbol and package view is quite commonly used by the manufacturers in their data sheets. These combinations are shown in Fig. 13.5a and b respectively.



(a) 8-lead metal can
(TO-99), top view

(a)



(b) 8-lead mini, dip
top view

(b)

Fig. 13.5: **Pin diagrams for a) metal can; b) 8-pin DIP package of op amp. (NC means no connection).**

The pin count of every IC including op amps is done as follows. Look at the top view of the IC and note the position of a notch or a dot in case of DIP and a tab in case of a metal can package. The first pin on the left hand side of the notch or dot or tab identifies the pin 1. Then other pins are counted counter-clockwise. If you see the IC in its bottom view, then this counting scheme is reversed. That is in bottom view, the next pin on the right side of the tab or dot is Pin 1 and the counting is done from 1 to 8 in clockwise direction.

SAQ 2 – Op amp IC pin identification

What is the way in which the IC pins are counted?

13.3.3 Number Code

On the packages of all the ICs, including op amps, some numbers are printed with the help of which the IC is identified. On op amp package, say in a typical IC, CA741C is printed. The first two letters 'CA' identify the manufacture's code. CA is the code for RCA, AD is for Analog Devices, LM is for National Semiconductor Corp, μA is for Fairchild, etc. The word 741C is the circuit designator for commercial purpose op amp. This word for any IC could be of three to seven numbers and letters. In 741C, C identifies the commercial

temperature range (0 to 70°C). Other temperature codes are I for industrial purpose (–25 to 85°C) and M for military purposes (–55 to 125°C).

SAQ 3 – Identifying op amp IC

Identify the details of the IC with number code LM 741M.

13.3.4 Power Supply

For supplying bias to a general purpose op amp IC (741C), a bipolar or dual power supply is required. Usually to power the op amp ICs, commercially available dual power supplies which give voltages ±15 V (plus and minus 15 V) or ± 9 V (plus and minus 9 V) are used. Two separate equal voltage sources with opposite polarities as shown in the Fig. 13.6 can also be used with a common terminal at ground (0 V) potential.

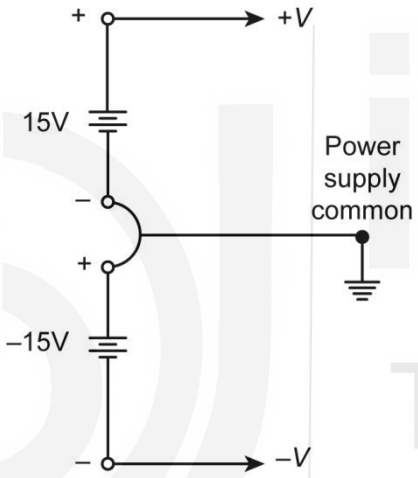


Fig. 13.6: **Dual power supply.**

SAQ 4 – Power supply connections to op amp IC

Name the pins of op amp 741C to which power supply is connected.

13.3.5 Precautions while Handling Op Amp IC

A circuit in which op amp is being used is built either on a breadboard or on a printed circuit board. There are certain precautions to be taken while constructing and using the circuit.

- While doing the entire wiring of the circuit keep the power supply off.
- Use wires of appropriate length. Avoid using too long wires.
- All ground connections should meet at a common electrical point.
- While starting the circuit, first of all, power (± *V*) should be supplied to the op amp.
- Apply signal to the input pins only after op amp is supplied with power.

- Always measure voltages and not currents. The current may be calculated by finding voltage at two ends of a resistor.
- When the work is over, remove signal first and then switch off the op amp power supply.

It is necessary here to stress further that **never**

- reverse the polarity of supply voltages given to IC pins;
- apply input signal voltages greater then + *V* and less than – *V*,
- connect any signal to input pins with op amp power supply off.

SAQ 5 – Op amp power supply

What happens if you connect positive terminal of the dual power supply to pin 4 and negative terminal to pin 7 of op amp 741C?

13.4 CHARACTERISTICS OF OP AMP

An op amp is a special type of amplifier possessing some very peculiar characteristics. In this section you will learn about some important characteristics of op amp which influence its performance, and make it a popular amplifier in various applications.

You must remember here that in the circuits fabricated using discrete or integrated components, the practical factors like power losses in devices, stray capacitances, temperature dependent behaviour of device parameters etc. affect the performance of the circuit. Hence, there is always a deviation in the parameter values from the ideal values for op amp. For example, an ideal operational amplifier has infinite voltage gain, infinite input impedance and zero output impedance. Actual characteristics of an op amp are as a matter of fact different.

Now we describe these characteristics in details.

13.4.1 Input-Output Relationship

As pointed out earlier, op amp amplifies the difference of voltage present between the non-inverting and inverting inputs (pins 3 and 2). If the difference voltage is V_D and the gain of the op amp is *A*, then the output voltage is AV_D. In Fig. 13.7, the voltage at pin 3 is designated to be V_1 and at pin 2 it is V_2. Thus

$$V_D = V_1 - V_2$$

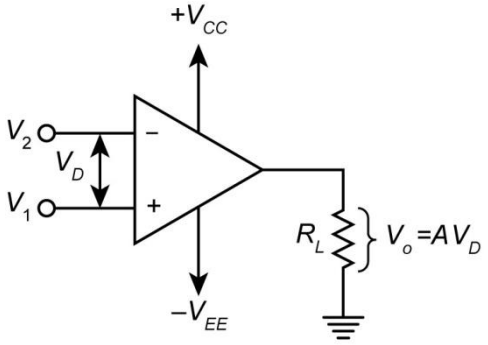


Fig. 13.7: **Output voltage depends on the input difference voltage.**

and the output voltage is

$$V_O = A(V_1 - V_2) = AV_D$$

This gives the voltage gain

$$A = \frac{V_O}{V_D} \qquad (13.1)$$

The voltage gain *A* in this equation is referred to by several names – large signal voltage gain (LSVG), open loop gain (A_{OL}) or differential voltage gain (A_D).

Remember that the difference voltage, V_D, has been calculated as follows:

(V_D) = voltage at non-inverting terminal, pin 3 (V_1) –
voltage at inverting terminal, pin 2 (V_2)

Both (V_1) and (V_2) are measured with respect to the ground. Note that the gain of the ideal operational amplifier is infinite, while in practice, say for μA 741C, the gain is 200,000. Thus theoretically, the output voltage should be 200,000 times (V_D). But we cannot obtain from any amplifier a voltage which is greater than the bias voltage supplied by the power supply. Therefore, the output voltage gets saturated, which is limited by the supply voltage. Actually, the op amp consists of several transistors across which certain voltages are dropped in order to maintain their proper functioning. This limits the output voltage below the supply voltage. The upper limit of the output voltage V_O is the positive saturation voltage, $+V_{SAT}$ and the lower limit is the negative saturation voltage, $-V_{SAT}$. In the case of the general purpose op amp biased with ±15 V power supply the $+V_{SAT}$ and $-V_{SAT}$ are +14 V and –13 V respectively restricting the peak-to-peak symmetrical swing to 13 V. You should remember that if the input to pin 3 is greater than that to pin 2, then V_D is positive and the output is $+V_{SAT}$. Now if the input to pin 2 is greater than that to pin 3, then V_D is negative and the output is $-V_{SAT}$.

SAQ 6 – Differential input voltages

How do you calculate input difference voltage of an op amp?

13.4.2 Voltage Transfer Curve

Fig. 13.8 shows a plot drawn (not to the scale), between the difference input voltage, V_D, and the output voltage, V_O. The curve in the plot is known as **voltage transfer curve**. If V_D is positive, V_O reaches $+V_{SAT}$ and if it is negative then V_O is $-V_{SAT}$. Thus output voltage cannot be greater than $+V_{SAT}$ and lesser than $-V_{SAT}$. If the plot is drawn to the scale, then the curve will be a vertical straight line for an ideal op amp.

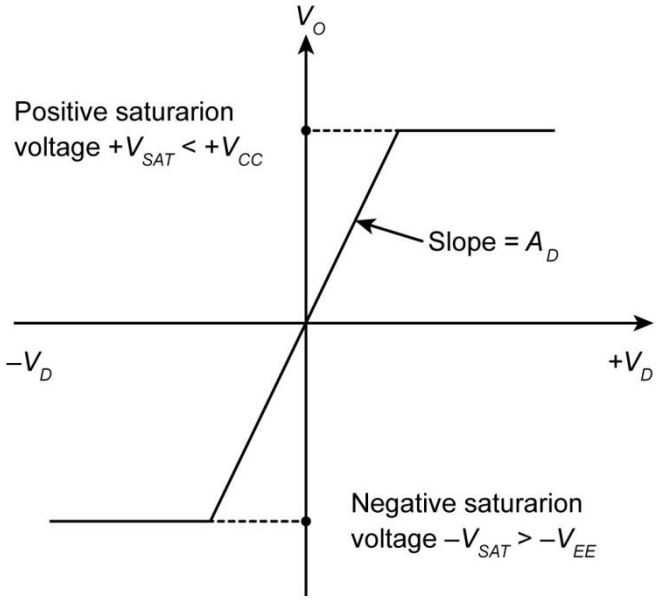


Fig. 13.8: **Ideal voltage transfer curve.**

13.4.3 Input Offset Voltage

Ideally the output of an op amp should be zero, when equal voltage is applied at both the inputs. However, in practical op amp, a small voltage difference is required between the two inputs to get 0 V output. **Input offset voltage** is the voltage which is necessary to be applied between pins 2 and 3 so as to get zero output at pin 6. If the dc input voltages applied to pins 3 and 2 are V_1 and V_2 as shown in Fig. 13.9, then the input offset voltage is $V_{IO} = V_1 - V_2$ for getting zero output voltage. The value of V_{IO} can be positive or negative. The smaller is the value of V_{IO}, better is the matching of the input terminals. For 741C, the maximum value of V_{IO} is 6 mV.

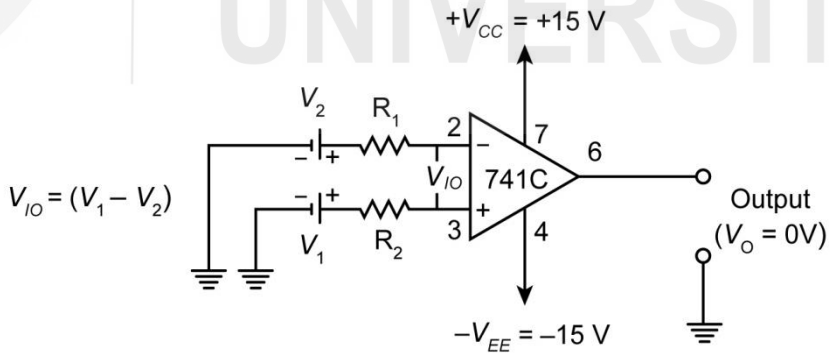


Fig. 13.9: **Measuring input offset voltage.**

SAQ 7 – Input offset voltage

If you wish to amplify an input differential voltage of 5 mV, can IC 741C be a good choice of op amp?

13.4.4 Output Offset Voltage

Output voltage of an op amp should be ideally zero when both the inputs are at the same potential, zero or grounded. However, in practice some output

voltage may be available with both the inputs grounded. This voltage is known as **output offset voltage** and it should be made zero, otherwise, the results will be inaccurate.

To reduce the output offset voltage to zero in IC 741C, a carbon potentiometer of high resistance, say 22 kΩ, is connected between the pins 1 and 5, and the wiper is connected to pin 4 ($-V_{EE}$ V) as shown in Fig. 13.10. Adjust the position of the wiper so that output offset voltage is reduced to zero.

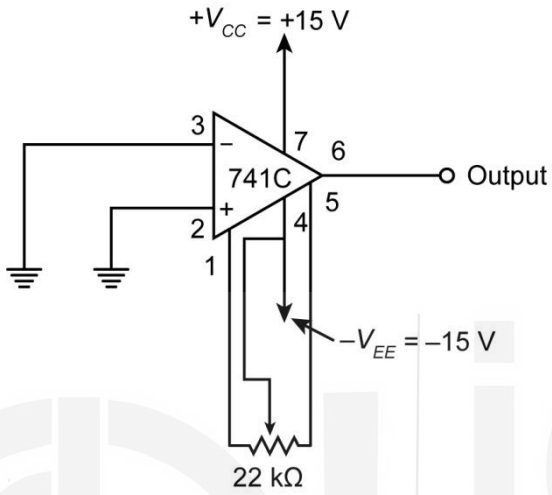


Fig. 13.10: **Adjusting output offset voltage.**

SAQ 8 – Output offset voltage

What is the output offset voltage? Why is it necessary to be reduced to zero?

13.4.5 Input Impedance

Input impedance or differential input resistance, R_I of an op amp is the equivalent resistance which can be measured at either of the inputs – inverting or non-inverting – with the other terminal grounded. Ideally this resistance is infinite. But in case of 741C, R_I is about 2 MΩ.

In many op amps the transistors T_1 and T_2 are field effect transistors (FETs) rather than bipolar junction transistors (BJTs). Advantage of using FET is that there is no base current required to operate this circuit. Hence it can provide a high input impedance to op amp avoiding any loading of the signal source.

13.4.6 Output Resistance

Output resistance, R_O is the equivalent resistance measured between the output pin 6 and the ground. Ideally the value of R_O is zero, but for 741C it is 75Ω.

13.4.7 Common Mode Rejection Ratio (CMRR)

There may be situations when the op amp is being used in an electrically noisy environment. The pins 2 and 3 may pick up same noise voltage. The op

amp amplifies the difference in voltages at the two inputs, therefore with the same voltage present at the two inputs the output voltage due to noise should be ideally zero thus cancelling unwanted noise singles. To assess whether both the inputs are properly matched for this purpose a term known as **common mode rejection ratio** (**CMRR**) is used. It is defined as the ratio of the open loop voltage gain, A_{OL}, to the common mode voltage gain, A_{CM}.

$$\text{CMRR} = \frac{A_{OL}}{A_{CM}} \qquad (13.2)$$

The common mode voltage gain, A_{CM}, is measured using the circuit shown in Fig. 13.11.

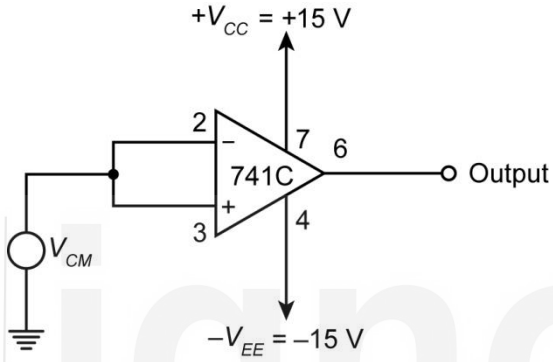


Fig. 13.11: **Common mode connections.**

Both the inputs are connected to each other and given the same common mode voltage, V_{CM} and the common mode output voltage V_{OCM} is noted. Then the common mode voltage gain is

$$A_{CM} = \frac{V_{OCM}}{V_{CM}}$$

Then CMRR can be calculated using Eq. (13.2). Ideally, CMRR should be infinite, since open loop gain (A_{OL}) is infinite. However, in practice for IC 741C, A_{OL} is 200,000 and its CMRR is 90 dB.

SAQ 9 **– CMRR**

Is it preferable to use an op amp with low CMRR? Why?

13.4.8 Slew Rate

Slew rate indicates how rapidly the output of an op amp changes with the change in the input signal. It is defined as the maximum rate of change of output voltage (in volts) per unit time (in micro seconds). Thus

$$\text{SR} = \left.\frac{dV_O}{dt}\right|_{\max} \text{V}\mu\text{s}^{-1}$$

Slew rate is normally specified by the manufacturer at the unity closed loop gain (+1). Ideally the slew rate should be infinite. For IC 741C, the slew rate is 0.5 $\text{V}\mu\text{s}^{-1}$ which limits its use at higher frequencies. For use at higher frequencies special purpose op amp like LM 318 is used. It has a slew rate of 70 $\text{V}\mu\text{s}^{-1}$.

EXAMPLE 13.1: THE SLEW RATE

The slew rate of an op amp is 1 $V\mu s^{-1}$. If a triangular wave of $\pm$ 5V is to be obtained at the output of the op amp, what is the maximum frequency of the signal that can be applied at the input?

SOLUTION ■ The triangular wave signal of $\pm$ 5V is shown in Fig. 13.12. The signal travels from – 5V to + 5V and back to – 5V in one cycle of the signal.

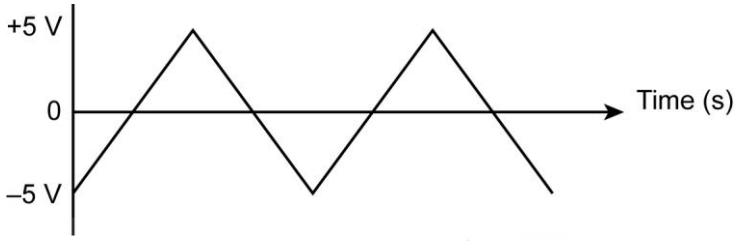


Fig. 13.12: **Triangular wave of ± 5V amplitude.**

Hence the total voltage traversed by the output of an op amp will be 20 V (Rising edge from – 5V to + 5V and falling edge from + 5V to – 5V).

The slew rate of op amp is 1 $V\mu s^{-1}$. Hence to traverse 20 V (i.e. to complete one cycle), it will take 20 μs. This is the shortest period of the signal wave that can be handled. We can obtain the frequency of this signal.

$$f_{max} = \frac{1}{\text{Time period}} = \frac{1}{20\ \mu s} = 50\ \text{kHz}$$

Hence, the maximum frequency of the signal that can be faithfully obtained, without any distortion at the output will be 50 kHz.

From this example, you must have understood how the frequency of signal handled by the op amp is limited by the slew rate.

13.4.9 Maximum Output Current

Maximum output current for ideal op amp is infinite. This current flows from the op amp IC when the output terminal is shorted to the ground. But this will damage the practical op amp. To avoid this damage all op amps of 741 family have built-in protection circuitry and are protected up to 25 mA of current. Therefore, its maximum output short circuit current is 25 mA.

13.4.10 Power Consumption

The amount of power that is consumed by an op amp to operate properly (with zero input voltage) is defined as the power consumption of the op amp. For 741C, it is 85 mW. This op amp also draws a current of 2.8 mA from the power supply.

13.4.11 Gain-Bandwidth Product

Ideally the operational amplifier has infinite bandwidth, but as the closed loop gain is increased the bandwidth decreases. Normally it is defined as the bandwidth of the op amp when its closed loop gain is 1. For 741C, the gain bandwidth product (GB) is approximately 10^6. Hence under unity gain, the bandwidth is 1 MHz.

13.4.12 Comparison of Ideal Op Amp and 741C

In Table 13.1 we summarize the comparison of ideal values of various op amp characteristic parameters with IC 741C.

Table 13.1: Comparison of Ideal Op Amp Parameters with IC 741C

Sl. No.	Parameter	Ideal Op amp	741C
1.	Open loop voltage gain (A_{OL}, A_D).	Infinite	200,000
2.	Input impedance (R_I)	Infinite	2 MΩ
3.	Output resistance (R_O)	Zero	75 Ω
4.	Output offset voltage	Zero	6 mV
5.	Common mode rejection ratio (CMRR)	Infinite	90 dB
6.	Slew rate	Infinite	0.5 $V\mu s^{-1}$
7.	Bandwidth (BW)	Infinite	1 MHz.

13.4.13 Equivalent Circuit of an Op Amp

The equivalent circuit of an op amp is shown in Fig. 13.13. In the circuit R_I and R_O are input and output resistances of the op amp and AV_D is the equivalent Thevenin voltage source. The value of A, R_I and R_O are available from the manufacturer's data sheet.

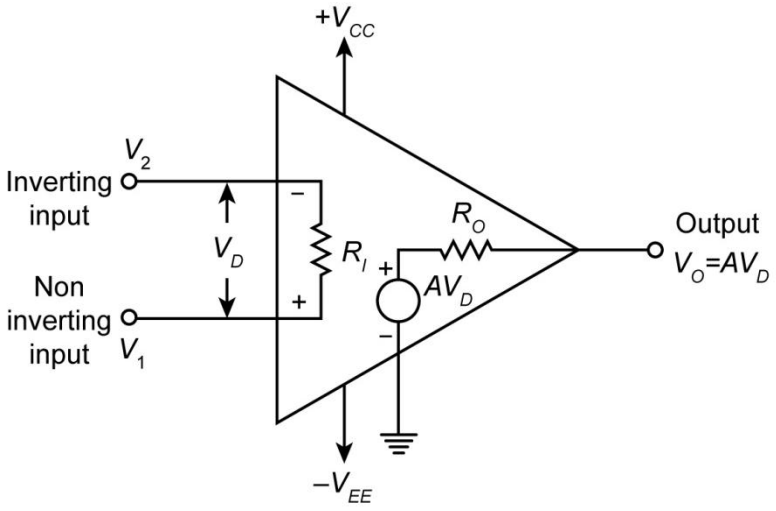


Fig. 13.13: **Equivalent circuit of an op amp.**

Let us now summarise the points discussed in this unit.

13.5 SUMMARY

Concept	Description
Building blocks of op amp	■ Op amp has two inputs and single output. Differential amplifier is the first stage of op amp whereas push pull power amplifier is the last stage.
Op amp IC number codes	■ The name of the manufacturer, the op amp and temperature range can be found out by reading the number code printed on the top of the IC package.
Power supply requirement	■ A dual power supply is needed to operate the op amp. We connect positive voltage to pin 7 and negative voltage to pin 4.
Ideal op amp characteristics	■ The ideal operational amplifier has infinite voltage gain, input resistance, CMRR and slew rate. It has zero output resistance and output offset voltage.

13.6 TERMINAL QUESTIONS

1. Draw the pin-out diagram of bottom view of op amp 741C in dual in-line pack.
2. Why is it necessary to provide the power supply to the op amp before applying the signal to an op amp circuit?
3. What will be the lowest value of load resistance that can be handled by IC 741C op amp if the output voltage is + 10V?

13.7 SOLUTIONS AND ANSWERS

Self-Assessment Questions

1. Inverting input pin 2, non-inverting input pin 3 and the output pin 6.
2. See the top view of the IC. Look for the notch or dot on the body of the IC. The pin on the left of the notch or dot is pin 1. Then start counting pins in counter-clockwise direction.
3. For the IC with number LM741M, the letters LM identify the name of the manufacturer, National Semiconductor Corp. The letters 741 indicate op amp. The letter M indicates the temperature range for the Military Standards, i.e. –55° to 125°C. Thus, LM 741M means that it is an op amp manufactured by National Semiconductor Corp, for military purpose to be used in the temperature range of –55° to 125°C.
4. Pins 4 and 7. Negative voltage is connected to pin 4 and positive voltage is connected to pin 7.
5. It will permanently damage the op amp.

6. Input difference voltage to an op amp V_D is calculated as follows:

$$V_D = \text{voltage at pin 3 } (V_1) - \text{voltage at pin 2 } (V_2)$$

where the voltages at pins 2 and 3 are measured separately with respect to the ground potential (0 V).

7. No. The input offset voltage of IC 741C is 6 mV. Hence the differential voltage of smaller than 6 mV cannot be amplified faithfully, unless an additional V_{IO} for this IC is applied at the inputs alongwith the input signal.

8. It is the voltage available at the output pin 6 even when both the input pins 2 and 3 are grounded. If it is not reduced to zero, then any reading taken at the output pin will always have this excess dc voltage riding on the real output voltage; and we will get faulty results.

9. No. Higher is the CMRR, better is the matching of input terminals and immunity against noise common on both inputs.

Terminal Questions

1. Refer to Fig. 13.14.

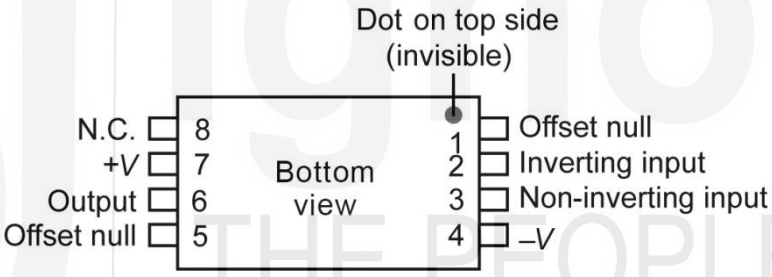


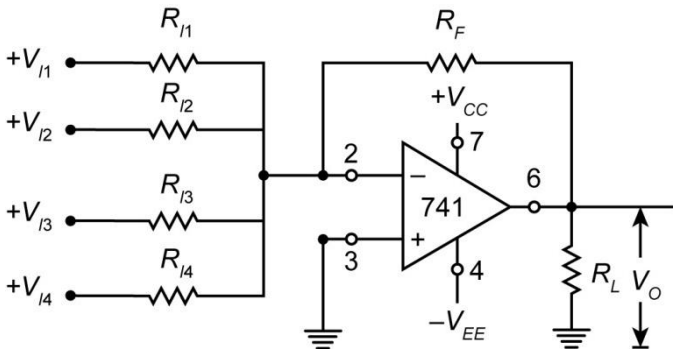
Fig. 13.14: **Bottom view pin out diagram of IC 741C DIP.**

2. When op amp is connected in a circuit, it is always necessary to bring it first into operation by applying it the supply voltage. Once it stabilizes, then the input signal should be provided. When the supply voltages are not provided to the op amp IC, the internal components like transistors are not properly biased. In such situation if the signal is given to the input pins, that can damage the internal components and make the IC non-functional.

3. The maximum output current supplied by IC 741C is 25 mA. When output voltage = 10 V, the minimum load resistance that can be connected to the output

$$= \frac{10\text{ V}}{25\text{ mA}} = 400\ \Omega.$$

Hence loads larger than 400 Ω can be used for 10 V output voltage. Note that, if the output voltage is larger, the required value of load resistor will also be larger.



In this figure an adder using op amp is shown. Op amp can be used for various mathematical operations on analog signals, as you will learn in this unit.

UNIT 14

APPLICATIONS OF OPERATIONAL AMPLIFIER

Structure

STUDY GUIDE

In the last unit you learnt about the fundamentals of operational amplifier. Due to its special characteristics, this device is useful in performing different functions. In this unit you will learn about various applications of op amp. These applications may or may not involve any feedback circuit, but a negative feedback empowers op amp to perform different mathematical operations. To understand these feedback circuits, you should revise your knowledge of negative feedback that you learnt in Unit 10 of this course. There are several Design Examples, SAQs, Terminal Questions given in this unit. You should solve them on your own to get better grasp of the topic.

"Op amp's popularity stems from its versatility."

G.B. Clayton

14.1 INTRODUCTION

In the last unit you learnt about the special properties of operational amplifier like extremely high gain, high input impedance, low output resistance, etc. These characteristics of the op amp make it a very useful component of many application circuits like comparators, adders, multipliers, etc.

We will begin with an important application of op amp as a comparator which generates a saturated output voltage ($+V_{SAT}$ or $-V_{SAT}$) by comparing the signals applied at the inputs. Such comparators are used in different applications like automatic door openers, automatic light switches, product pieces counters on the conveyor belt in a factory etc. The comparators and their applications in electronic circuits are explained in Sec. 14.2.

You have learnt the concept of feedback and applications of negative feedback in the previous block of this course. In operational amplifier we can use the negative feedback to perform many important tasks. In Section 14.3 to 14.7 you will learn about different circuits like inverting amplifier, non-inverting amplifier, adder / subtractor, basic differentiator and basic integrator.

We will explain the working of all these circuits and you will also learn to design these circuits with required input-output relationships. In all these circuits we will make use of IC 741C, the general purpose op amp IC. You were familiarized with its characteristics in the last unit.

Expected Learning Outcomes

After studying this unit, you should be able to:

- explain the working of op amp as a comparator;
- design a voltage level detector and a zero crossing detector;
- draw the circuit diagram of the inverting amplifier and obtain its closed loop gain, A_{CL} ;
- describe the concept of virtual ground in op amp;
- use an inverting amplifier as a multiplier or divider;
- design an inverting amplifier with a particular gain;
- draw a circuit diagram of a non-inverting amplifier and obtain its closed loop gain;
- draw a circuit diagram of an inverting adder;
- design a subtractor using the combination of inverting and non-inverting amplifiers;
- draw the circuit diagram of a basic differentiator and obtain the expression for its output; and
- draw the circuit diagram of a basic integrator and obtain the expression for its output.

14.2 OP AMP AS A COMPARATOR

The op amp has very large gain and hence any small difference between the voltages applied at the inverting and non-inverting inputs drives the output of the amplifier to its saturation value. If the voltage at the non-inverting input

(V_{NI}) is more positive than that at the inverting input (V_{INV}) then the output is $+V_{SAT}$ and if it is lower than the inverting input, then the output is $-V_{SAT}$.

We can make use of this feature of the op amp to design a comparator circuit. By comparing the voltage levels at the two inputs, we can obtain the output. Such output can be used in many practical applications.

Now we describe the use of op amp comparator as a voltage level detector.

14.2.1 Voltage Level Detector

In Fig. 14.1 we have shown a circuit for an op amp used a comparator. A fixed reference voltage V_{REF} is applied to inverting input pin 2. The time dependent signal V_{in} is applied to the non-inverting input pin 3. The output voltage V_O depends on the voltage difference V_D between the two inputs.

$$V_O = A.(V_{NI} - V_{INV})$$
$$= AV_D = A(V_{in} - V_{REF})$$

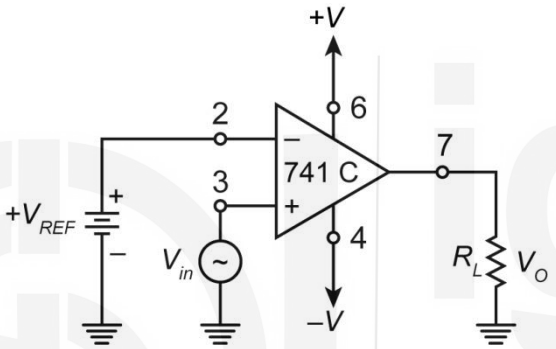


Fig. 14.1: **Op amp as a voltage level detector.**

If the reference voltage applied to inverting input is (say) 1 V, then for $V_{in} = 1\text{V}, V_D = 0$. Hence $V_O = 0$ as shown in Fig. 14.2. If $V_{in} > 1\text{V}$ then V_D is positive. In this case the output gets limited to $+V_{SAT}$ as shown in Fig. 14.2. If $V_{in} < 1V$, then V_D is negative which limits the output to $-V_{SAT}$.

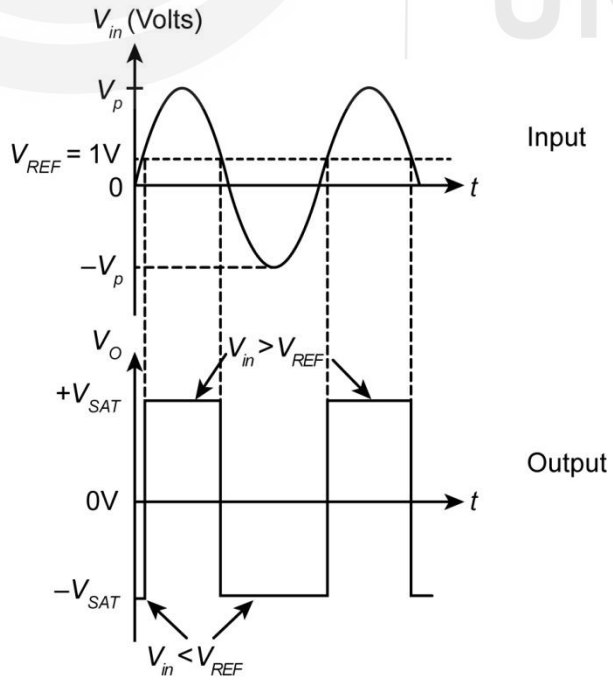


Fig. 14.2: **Input and output waveforms of a non-inverting comparator with reference voltage $V_{REF} = 1\text{V}$.**

Thus at any instant of time the output voltage V_O shows whether the input is greater than V_{REF} or less than V_{REF}. This circuit acts like an analog to digital converter. This **non-inverting comparator** is also known as **voltage level detector**. The value of V_{REF} can be 0, or any value positive or negative. V_{REF} can be connected to any of the inputs. However, to find the output waveform, you must note whether V_D is positive or negative. If the reference voltage V_{REF} is connected to the non-inverting input pin 3 and the input signal is given to pin 2, the comparator is known as **inverting comparator**.

14.2.2 Zero Crossing Detector

Another application of comparator is the zero crossing detector. Fig. 14.3 shows a circuit for zero crossing detection.

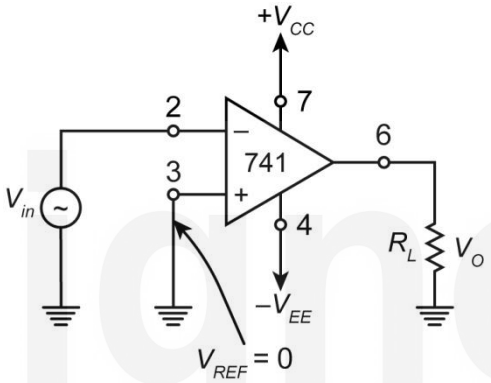


Fig. 14.3: **Zero crossing detector in inverting comparator mode.**

Here pin 3 is grounded making the ground potential (0 V) to be the reference voltage. The input signal is given to pin 2. This is in the inverting comparator mode. When the V_{in} exceeds 0 V, then V_D is negative and the V_O is limited to $-V_{SAT}$. Likewise, when V_{in} is less than 0 V, then V_D is positive and the output, V_O is limited to $+V_{SAT}$. Thus the output voltage shows whether the input voltage is above or below the zero level as is shown in Fig. 14.4.

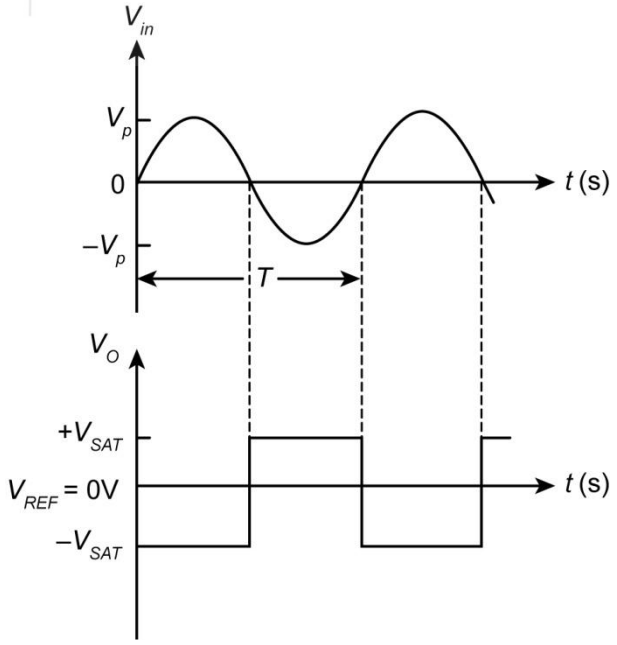


Fig. 14.4: **Input and output waveforms of a zero crossing detector of Fig. 14.3.**

SAQ 1 – Zero crossing detector

Trace the output voltage waveform of the circuit given in Fig. 14.5, where a triangular wave is given to the inverting input terminal.

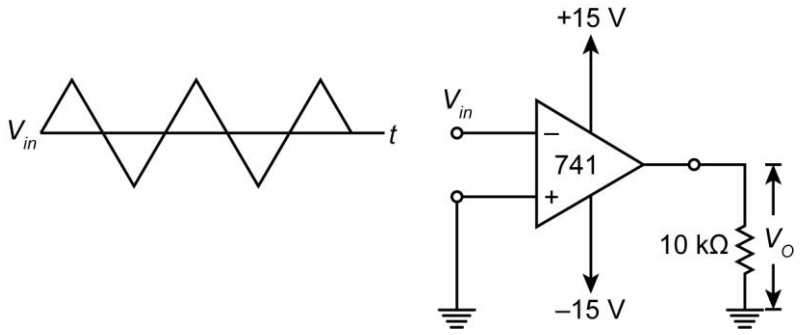


Fig. 14.5: **Waveforms of zero crossing detector.**

After discussing about the use of op amp as a comparator, now we describe the applications of op amp using negative feedback.

14.3 NEGATIVE FEEDBACK IN OP AMP

While using the op amp as a comparator, we used its property of infinite open loop gain. However, if we can control the gain of the op amp, then many more other applications of op amp can be implemented.

In Unit 10 on Amplifiers you learnt that negative feedback reduces the gain of an amplifier. Negative feedback can be obtained if the signal fed back from the output is in opposite phase of the input signal. In op amp, you know that the inverting input is in opposite phase of the output. Hence, if we feed a part of the output signal to this input through a feedback network, we can achieve the negative feedback configuration of an op amp circuit. Fig. 14.6a and b show the two possible configurations of op amp negative feedback circuits.

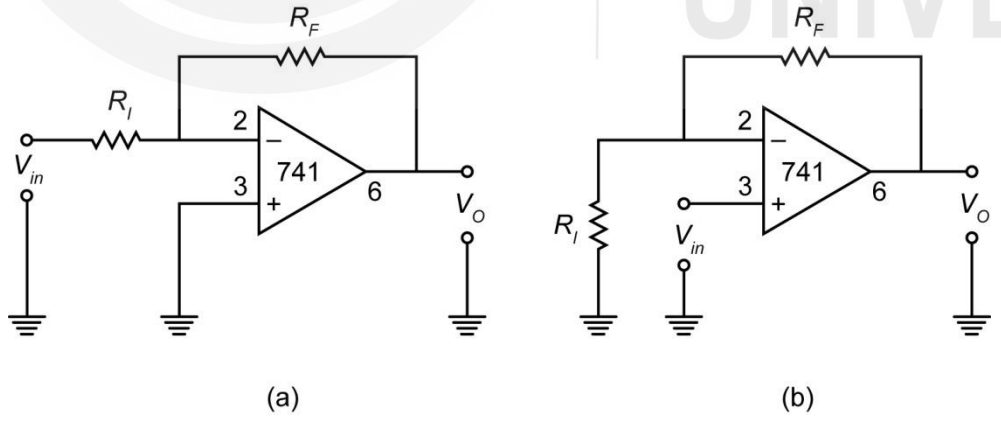


Fig. 14.6: **Negative feedback circuits of op amp with input given to a) inverting input; b) non-inverting input.**

In both these circuits, the feedback is given to the inverting input through a feedback resistor R_F. In certain applications, this resistor may be replaced by another device like capacitor, as you will find while learning about integrator circuit shortly.

Before going further to learn about the applications of op amp with negative feedback, attempt an SAQ.

SAQ 2 – Feedback in op amp

What will happen if you apply the feedback to the non-inverting input?

14.4 INVERTING AMPLIFIER

Consider the circuit shown in the Fig. 14.7. In this circuit the output pin 6 is connected through a resistor R_F to the inverting input pin 2. The input voltage is given to pin 2 through an input resistor R_I. The non-inverting input pin 3 is grounded. This is similar to the circuit shown in Fig. 14.6a. The output pin 6 is also grounded through the load resistor R_L.

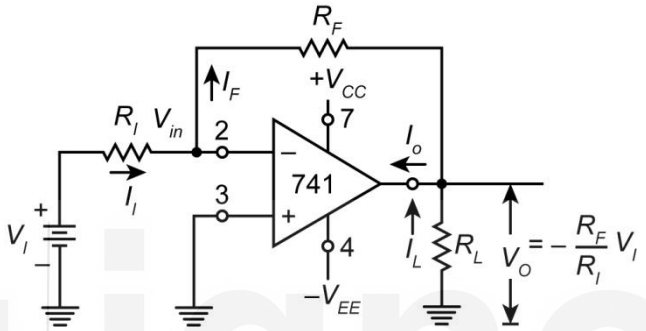


Fig. 14.7: **Inverting amplifier.**

To analyze this circuit, we make two assumptions based on the properties of ideal op amp.

a) Due to infinitely large gain of the op amp, the finite output (lesser than V_{SAT}), is obtained only if the difference between the inputs (V_D) is zero.

b) The input impedance of op amp is infinite, hence no current flows into the input terminals of the op amp.

Although, these assumptions are based on the ideal op amp characteristics, even for practical op amps these are applicable quite satisfactorily.

A positive input voltage $(+V_I)$ is applied to the inverting $(-)$ input pin 2 through input resistor R_I and the feedback resistor R_F provides the necessary feedback from the output to the input. The non-inverting input is at ground potential (0 V). As per the first assumption, because non-inverting (+) input (pin 3) is grounded, pin 2 is also at ground voltage (0 V). Thus though pin 2 is not connected to the ground, yet it appears to be grounded. Therefore, the inverting input is said to be at **virtual ground**. You must remember that because of virtual ground, under negative feedback, the inverting terminal always remains at the same voltage, as that at the non-inverting terminal. This is very important concept and will come handy to analyse all negative feedback op amp circuits.

In the circuit of Fig. 14.7, the current through R_I is decided by the voltage drop across it. One end of R_I is connected to $+V_I$ and another end is at 0 V due to virtual ground concept. Therefore, the voltage drop across R_I is $+V_I$. The input current, I_I, flowing through R_I from a point of higher potential to a point of lower potential (i.e. pin 2 which is at 0 V) is

$$I_I = \frac{V_I}{R_I} \qquad (14.1)$$

Now, as per our second assumption, no current can enter the op amp. Therefore I_I has to flow through R_F. Therefore, I_F, the current flowing through R_F is equal to I_I. That is $I = I_I = I_F$. Thus the voltage drop across R_F is

$$V_F = IR_F \qquad (14.2)$$

Putting for I from Eq. (14.1) we get

$$V_F = \frac{V_I}{R_I} R_F \qquad (14.3)$$

Since pin 2 is at virtual ground, R_L is in parallel with R_F. Therefore, the magnitude of V_F is equal to V_O. But V_F is negative because the current flows from pin 2 (which is at 0 V) to pin 6. Thus, V_O the voltage between pin 6 and ground is

$$V_O = -V_F$$

$$= -\frac{V_I}{R_I} R_F = -\frac{R_F}{R_I} V_I \quad \text{(using Eq. 14.3)}$$

The closed loop gain of the amplifier, A_{CL}, is

$$A_{CL} = \frac{V_O}{V_I} = -\frac{R_F}{R_I} \qquad (14.4)$$

Thus A_{CL} depends on R_F and R_I only and does not depend on the open loop gain of the operational amplifier. Since A_{CL} is negative, this configuration of the amplifier is called **inverting amplifier**. The choice of R_F and R_I is in the hands of the designer and the gain of practically any value can be obtained. In all practical applications the value of R_I should be chosen to be large, say 10 kΩ, so that it does not short out the input resistance of the op amp.

The output current I_O is sum of the current I flowing through R_I and the current $I_L = V_O / R_L$ flowing through the load R_L. Thus

$$I_O = I + I_L \qquad (14.5)$$

While designing an op amp based amplifier, the amount of current available at the output should also be kept in mind. For example, for IC 741C, maximum output current is 25 mA. The value of I is set by V_I and R_I. Hence, the load current (determined by V_O / R_L) should be restricted by choosing sufficiently large value of R_L.

The inverting amplifier circuit can be used for multiplication and division. The output voltage is R_F / R_I times the input voltage. If the input voltage represents some number then the output voltage will be equal to that number multiplied by the factor R_F / R_I. The ratio R_F / R_I is under our control and can assume any value. With $R_F > R_I$ we can use the inverting amplifier for multiplication. By making R_I greater than R_F it can be used for division.

EXAMPLE 14.1: INVERTING AMPLIFIER

Design an amplifier using op amp 741C with V_I of 1 V for a gain of –8 and I_O of 0.9 mA.

SOLUTION ■ Let us choose R_I = 10 kΩ.

Now, magnitude of gain $|A_{CL}| = \frac{R_F}{R_I}$

With $A_{CL} = -8$.

$$R_F = 8R_I = 80\,\text{k}\Omega$$

Using Eq. (14.1)

$$I = \frac{V_I}{R_i} = \frac{1\text{V}}{10\,\text{k}\Omega} = 0.1\text{mA}$$

From Eq. (14.5)

$$I_L = I_O - I = 0.9\,\text{mA} - 0.1\text{mA} = 0.8\,\text{mA}$$

For $V_I = 1\text{V}$, with gain = – 8,

$$V_O = 1\text{V} \times (-8) = -8\text{V}$$

$$I_L = \frac{V_O}{R_L}$$

$$\therefore \quad R_L = \frac{V_O}{I_L} = \frac{8\text{ V}}{0.8\,\text{mA}} = 10\,\text{k}\Omega$$

Hence, for the required circuit, $R_I = 10\,\text{k}\Omega$, $R_F = 80\,\text{k}\Omega$ and $R_L = 10\,\text{k}\Omega$. The dc bias for the op amp should be well above the expected output. In this example V_O is –8V, therefore a ±9V power supply will not be a good choice, because –8V would be just equal to $-V_{SAT}$. Therefore, a greater value of power supply is chosen, ±10V or above.

Now attempt an SAQ.

SAQ 3 – Inverting amplifier

What is the output voltage of the circuit given in Fig. 14.8 for specified input?

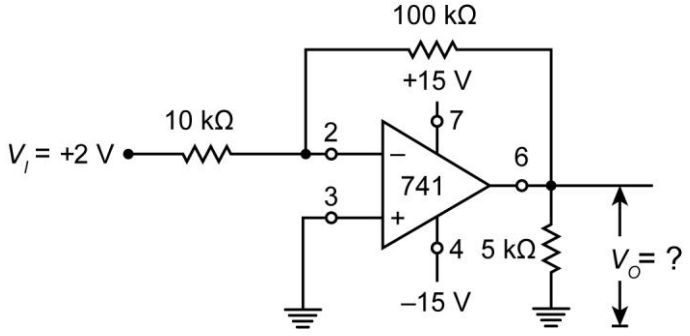


Fig. 14.8: **Output of an inverting amplifier.**

14.5 NON-INVERTING AMPLIFIER

The circuit given in Fig. 14.9 is for a non-inverting amplifier. You must have noticed that it is similar to the circuit shown in Fig. 14.6b. In this circuit R_I continues to be connected as in the case of inverting amplifier except that it is connected to ground and the input voltage V_I is given to the non-inverting (+) input at pin 3.

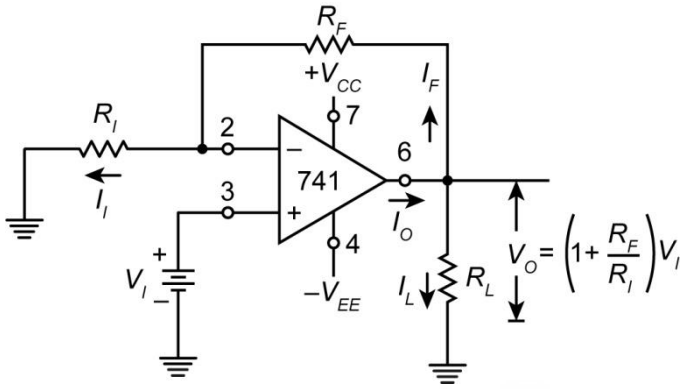


Fig. 14.9: **Non-inverting amplifier.**

As discussed in the last section, due to virtual ground, the inverting input pin 2 is also at the same voltage at which non-inverting input pin 3 is. Thus, pin 2 is at V_I which sets the current I_I through R_I. The voltage drop across R_I, being V_I, we get

$$I_I = \frac{V_I}{R_I} \qquad (14.6)$$

Obviously, I_I flows from pin 2 to the ground. Since no current flows in the op amp, I_F the current flowing through R_F has to be equal to I_I, i.e. $I = I_I = I_F$. Thus, the current I flows from output terminal pin 6 to pin 2 to ground. Hence, the output pin 6 is at a greater potential than pin 2. Since the load resistor R_L is now in parallel with the series combination of R_I and R_F therefore the output voltage is equal to the sum of voltage across R_I and R_F. Thus

$$V_O = V_I + IR_F$$

$$= V_I + \frac{V_I}{R_I}R_F \qquad \text{(using Eq. 14.6)}$$

Or the closed loop gain of the amplifier is

$$A_{CL} = \frac{V_O}{V_I} = \left(1+\frac{R_F}{R_I}\right) \qquad (14.7)$$

You must have noticed that A_{CL} has the same sign as the input voltage V_I i.e. positive. For this reason, we call this amplifier a **non-inverting amplifier**. In this case also the gain depends upon the values of R_F and R_I and not on the parameters of the operational amplifier. Remember that here the gain is always greater than unity. The ratio R_F / R_I can be made as small as possible and the gain can be made close to unity, but it can never be less than unity. Pin 6 being at a potential greater than the ground potential, the load current I_L flows from pin 6 to ground through the load resistor R_L.

EXAMPLE 14.2: NON-INVERTING AMPLIFIER

Design an amplifier using op amp 741C with V_I of 0.2V for a gain of +10 and I_O of 0.1 mA.

SOLUTION ■ Choose R_I = 10 kΩ.

Given $A_{CL} = +10 = 1 + (R_F / R_I)$

or $R_F / R_I = 10 - 1 = 9$

$\therefore$ $R_F = 9R_I = 90\,\text{k}\Omega$

$I = V_I / R_I = 0.2\,\text{V}/10\,\text{k}\Omega = 0.02\,\text{mA}.$

$V_O = +10V_I = 10 \times 0.2\,\text{V} = 2\,\text{V}$

From Eq. (14.5), $I_O = I + I_L$.

Substituting the values of I and I_O,

$0.1\text{mA} = 0.02\,\text{mA} + (V_O / R_L)$

$\therefore$ $V_O / R_L = (0.1 - 0.02)\,\text{mA} = 0.08\,\text{mA}$

Hence,

$R_L = 2\text{V}/0.08\,\text{mA} = 25\,\text{k}\Omega$

Hence, the components required for the given non-inverting amplifier are $R_I = 10\,\text{k}\Omega$, $R_F = 90\,\text{k}\Omega$ and $R_L = 25\,\text{k}\Omega$..

Before proceeding further, attempt an SAQ.

SAQ 4 – Non-inverting amplifier

What is the gain of the amplifier shown in Fig. 14.10?

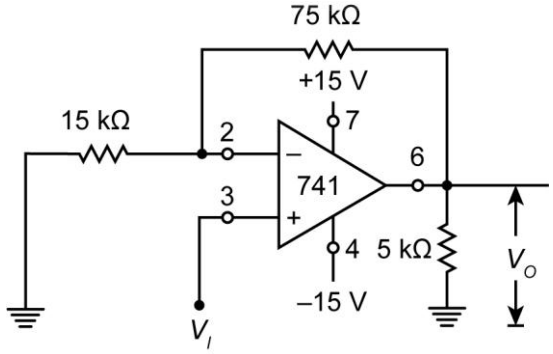


Fig. 14.10: **Gain of a non-inverting amplifier.**

14.6 ADDER / SUBTRACTOR

14.6.1 Inverting Adder

The inverting amplifier configuration of the op amp is useful in many applications. You already know that it can be used for multiplication and

division. The circuit of inverting amplifier shown in Fig. 14.7 has only one input through R_I. The number of inputs can be increased to any number. Consider the circuit given in Fig. 14.11 where three input voltages V_{I1}, V_{I2} and V_{I3} are connected to the inverting input (pin 2) through separate resistors R_{I1}, R_{I2} and R_{I3}. A single common R_F is used for all the R_I's.

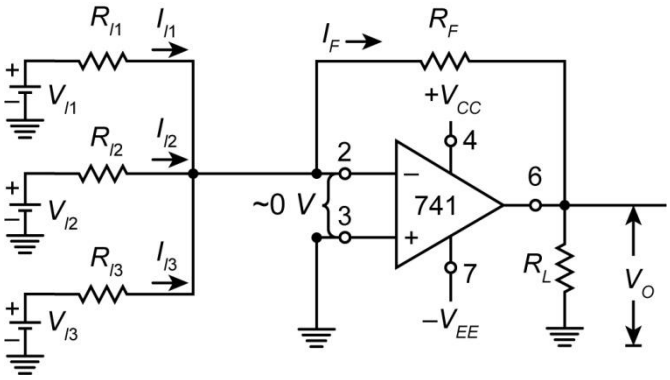


Fig. 14.11: **Inverting adder.**

Since pin 3 is grounded, pin 2 is at 0 V. The current flowing through R_F is the sum of all currents reaching the summing point at pin 2. These current are set by V_{I1} and R_{I1}, V_{I2} and R_{I2} and V_{I3} and R_{I3} respectively. Therefore,

$$I_F = I_{I1} + I_{I2} + I_{I3}$$

$$= \frac{V_{I1}}{R_{I1}} + \frac{V_{I2}}{R_{I2}} + \frac{V_{I3}}{R_{I3}}$$

The output voltage V_O is

$$V_O = -I_F R_F$$

$$= -\left(\frac{V_{I1}}{R_{I1}} + \frac{V_{I2}}{R_{I2}} + \frac{V_{I3}}{R_{I3}}\right) \times R_F \qquad (14.8)$$

And if all the resistors are of the same value, i.e. $R = R_F = R_{I1} = R_{I2} = R_{i3}$ then we get

$$V_O = -(V_{I1} + V_{I2} + V_{I3}) \qquad (14.9)$$

Thus the output of this circuit is the sum of all the input voltages. This circuit is known as *inverting adder*. The negative sign indicates 180° phase change between the input and the output.

If all the R_I's are chosen to be same (say R_I) and R_F is of different value then the output voltage will be

$$V_O = -\frac{R_F}{R_I} \times (V_{I1} + V_{I2} + V_{I3}) \qquad (14.10)$$

This equation indicates that the sum of the input is multiplied by a factor R_F / R_I which can be designed as per our requirement. In this equation if R_F / R_I is made equal to 1/3, then the resulting amplifier is an *averaging amplifier*.

The circuit of Fig. 14.11 has several applications. Apart from the applications mentioned above if the circuit is made with different values of R_I's, then Eq. (14.8) suggests that the output voltage is a weighted sum of all the outputs corresponding to each input. Such a circuit is used in digital to analog signal conversion, which is beyond the scope of this course. You may learn about it in your Master's programme.

EXAMPLE 14.3: INVERTING ADDER

Design and draw a 4-input channel inverting adder using op amp 741C with respective gains of –20, –15, –10 and –5 for the four inputs.

SOLUTION ■ We have to make a 4-input inverting amplifier circuit as shown in Fig. 14.12.

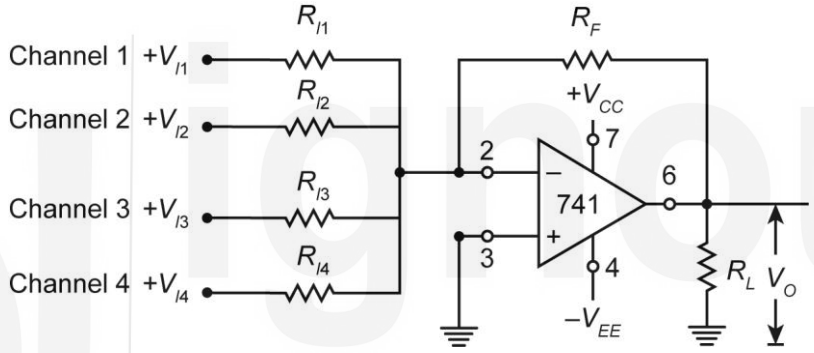


Fig. 14.12: **Four-input inverting adder.**

The Eq. 14.8 is rewritten for four inputs as follows:

$$V_O = -\left(\frac{V_{I1}}{R_{I1}} + \frac{V_{I2}}{R_{I2}} + \frac{V_{I3}}{R_{I3}} + \frac{V_{I4}}{R_{I4}}\right) \times R_F$$

$$= -\left(V_{I1}\frac{R_F}{R_{I1}} + V_{I2}\frac{R_F}{R_{I2}} + V_{I3}\frac{R_F}{R_{I3}} + V_{I4}\frac{R_F}{R_{I4}}\right) \qquad (14.11)$$

It is clear that the gain of each channel can be changed independently by changing the input resistor. We have

$$A_{CL1} = \frac{R_F}{R_{I1}},\ A_{CL2} = \frac{R_F}{R_{I2}},\ A_{CL3} = \frac{R_F}{R_{I3}},\ A_{CL4} = \frac{R_F}{R_{I4}}$$

Choose the value of R_I equal to 10 kΩ for the channel with the highest gain, i.e. for channel 1 with gain – 20, we take $R_{I1} = 10\,\text{k}\Omega$. Then the value of R_F can be found out by the relation

$$|A_{CL1}| = 20 = \frac{R_F}{R_{I1}} = \frac{R_F}{10\,\text{k}\Omega}$$

Thus, $R_F = 20 \times 10 = 200\,\text{k}\Omega$. Since R_F is common for all input channels, from this value of R_F we can find the values of R_I for other channels.

For channel 2, $|A_{CL2}| = 15 = 200 / R_{I2}$

or $R_{I2} = 200/15 = 13.33\,\text{k}\Omega$

For channel 3, $|A_{CL3}| = 10 = 200 / R_{I3}$

or $R_{I3} = 200/10 = 20\,\text{k}\Omega$

For channel 4, $|A_{CL4}| = 5 = 200 / R_{I4}$

or $R_{I4} = 200/5 = 40\,\text{k}\Omega$

The design result can be summarised as follows:

$R_F = 200\,\text{k}\Omega$

Channel	A_{CL}	R_I
1	–20	10 kΩ
2	–15	13.33 kΩ
3	–10	20 kΩ
4	–5	40 kΩ

Before going on to study the subtractor, attempt an SAQ based on the adder circuit.

SAQ 5 – Inverting adder

What is the output of the circuit shown in Fig. 14.13.

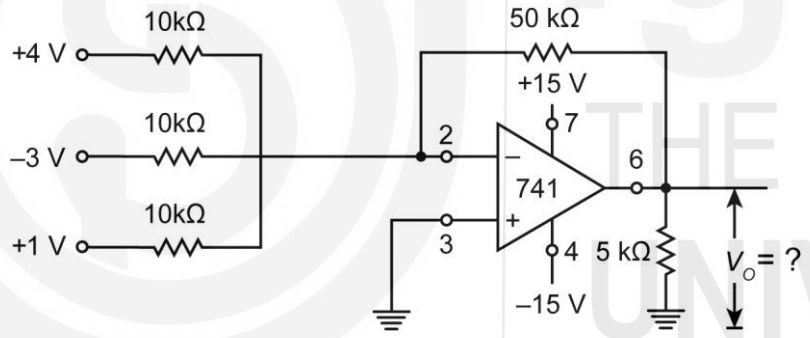


Fig. 14.13: **Output of an inverting adder.**

14.6.2 Differential Subtractor

We can use the differential configuration of op amp to obtain the subtraction of two signals. A simple circuit for getting the subtraction of two signals V_1 and V_2 is shown in Fig. 14.14.

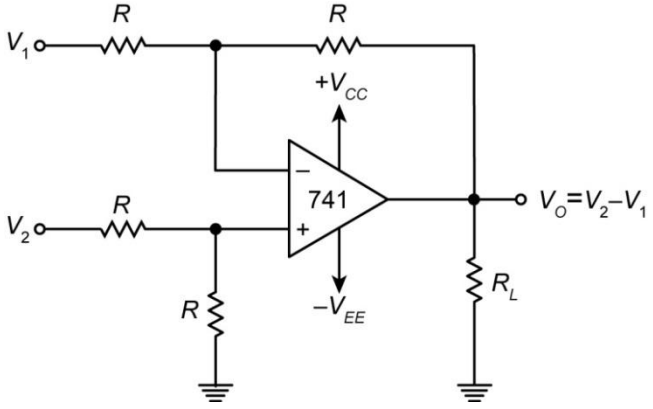


Fig. 14.14: **Subtractor using op amp.**

We can use the superposition method to obtain the expression for the output of this subtractor circuit. For this we apply voltage to one input terminal at a time and obtain the output due to that signal. Then we add the outputs due to both inputs and obtain the total resultant output.

When signal V_1 is applied to the inverting input (keeping V_2 = 0), the output V_{O1} is given by

$$V_{O1} = -\frac{R_F}{R_I} V_1$$

with $R_F = R_I = R$

$$V_{O1} = \frac{-R}{R} V_1 = -V_1$$

Now, if V_2 is applied to the non-inverting input (keeping V_1 = 0), the output V_{O2} is given by

$$V_{O2} = \left(1 + \frac{R_F}{R_I}\right) \times \text{(voltage at the non-inverting input)}$$

Voltage at the non-inverting input

$$= \frac{R}{R+R} V_2 = \frac{V_2}{2}$$

$$\therefore \quad V_{O2} = \left(1 + \frac{R_F}{R_I}\right)\left(\frac{V_2}{2}\right)$$

But $R_F = R_I = R$

$$\therefore \quad V_{O2} = V_2$$

$\therefore$ Total output of a subtractor

$$V_O = V_{O1} + V_{O2}$$

$$= -V_1 + V_2$$

Hence the circuit shown in Fig. 14.14 gives the difference (subtraction) of two input voltages.

14.7 BASIC DIFFERENTIATOR

Fig. 14.15 shows the circuit for basic differentiator which performs the mathematical operation of differentiation. The output waveform is the derivative of the input waveform.

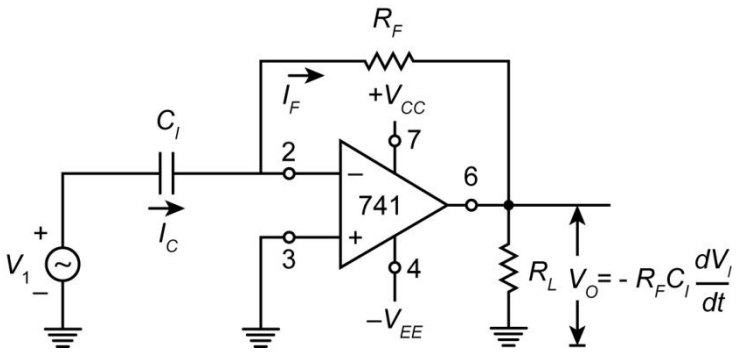


Fig. 14.15: **Basic differentiator.**

The differentiator circuit is obtained by replacing R_I of an inverting amplifier by a capacitor, while rest of the circuit remains the same. Just like in the case

of inverting amplifier, the current I_C flowing through the capacitor C_I should be equal to the current I_F flowing through the resistor R_F. Thus

$$I_C = I_F$$

The current I_C flows from the input signal source (V_I) to pin 2 from where it flows through R_F. Pin 2 being at 0 V due to virtual ground, the voltage drop across C_I is V_I and the drop across R_F is $-V_O$.

You can recall that the current flowing through a capacitor *C* is *C* times the rate of change of voltage across the capacitor. Therefore

$$I_C = C_I \frac{dV_I}{dt}$$

and $$I_F = -\frac{V_O}{R_F}$$

Since $I_C = I_F$,

$$C_I \frac{dV_I}{dt} = -\frac{V_O}{R_F}$$

Rearranging the terms, we get

$$V_O = -R_F C_I \frac{dV_I}{dt}$$

If the product $R_F C_I = 1$, then

$$V_O = -\frac{dV_I}{dt} \qquad (14.12)$$

Thus the output voltage is the negative derivative of the input voltage V_I. If the input is a sine wave, then the output waveform will be a negative of cosine wave; and if the input is a square wave, then the output will be a spike waveform; with 180° phase shift, as shown in the Fig. 14.16.

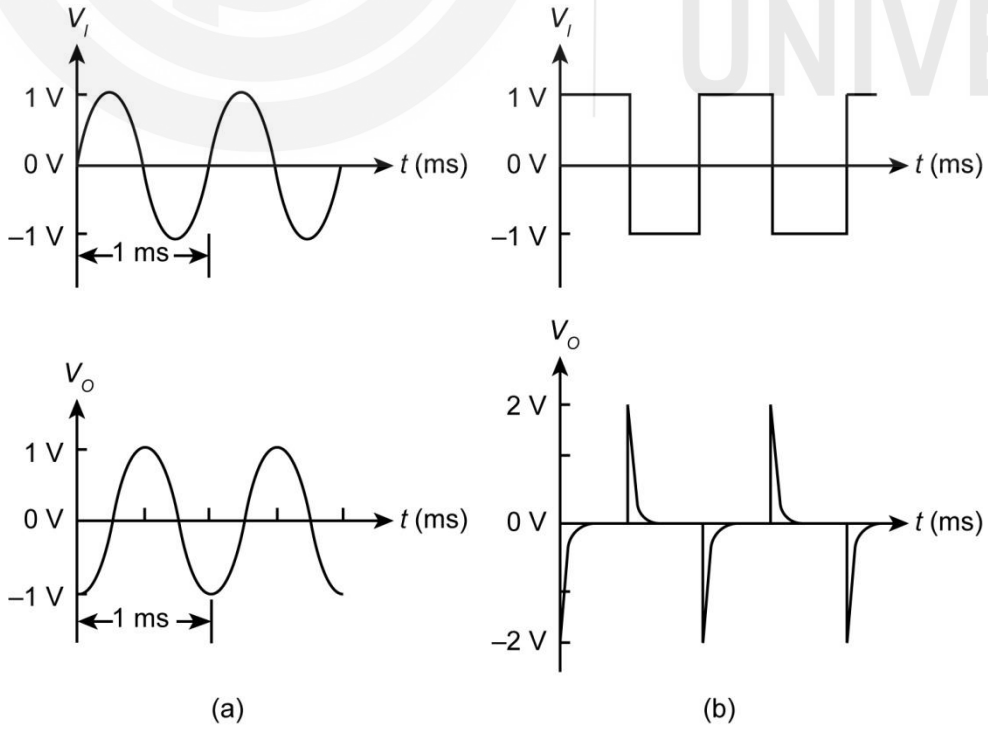


Fig. 14.16: **Output of a basic differentiator when input is a) sine wave; b) square wave.**

SAQ 6 – Basic differentiator

Draw the output waveform for the basic differentiator shown in Fig. 14.17.

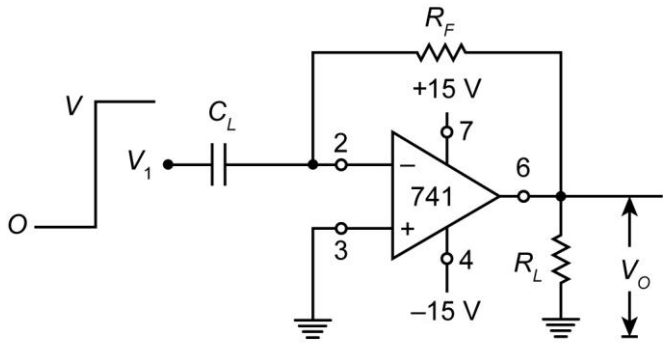


Fig. 14.17: **Response of basic differentiator to a step input signal.**

14.8 BASIC INTEGRATOR

Fig. 14.18 shows the circuit of a basic integrator which performs the mathematical operation of integration. The output waveform, V_O, is the integral of the input waveform, V_I.

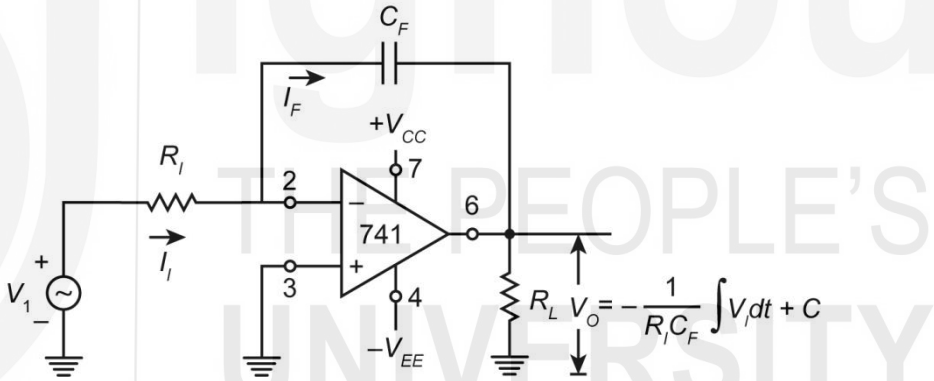


Fig. 14.18: **Basic integrator.**

The integrator circuit is obtained by replacing the resistor R_F by a capacitor C_F in the circuit of inverting amplifier, while rest of the circuit remains the same. Based on the basic assumptions made for negative feedback op amp circuits, the current I_I flowing through the resistor R_I has to be equal to the current I_F flowing through the capacitor C_F. Thus

$$I_I = I_F$$

Current I_I flows from the input signal generator to pin 2 and from there it flows through the capacitor C_F. Pin 2 being at 0V, the voltage drop across R_I is V_I and that across C_F is $-V_O$. Therefore,

$$I_I = \frac{V_I}{R_I}$$

and $$I_F = C_F \frac{d(-V_O)}{dt}$$

Hence we can write,

$$\frac{V_I}{R_I} = C_F \frac{d(-V_O)}{dt}$$

or

$$V_I = -R_I C_F \frac{d(-V_O)}{dt}$$

On integrating this equation, we get

$$\int V_I \, dt = -R_I C_F V_O$$

$$\therefore \quad V_O = -\frac{1}{R_I C_F} \int V_I dt \qquad (14.13)$$

Eq. (14.13) shows that the output is directly proportional to the integral of the input voltage waveform. If the product $R_I C_F$ is made equal to 1, then we get

$$V_O = -\int V_I \, dt \qquad (14.14)$$

If the input waveform is a sine wave then the output waveform is negative of inverted cosine wave, which means that it is a normal cosine wave as shown in Fig. 14.19a. If the input waveform is a square wave, then the output waveform is a triangular wave as shown in Fig. 14.19b. Here it is assumed that the $R_I C_F$ product is 1.

You know that for a sine wave

$$\int \sin x \, dx = -\cos x$$

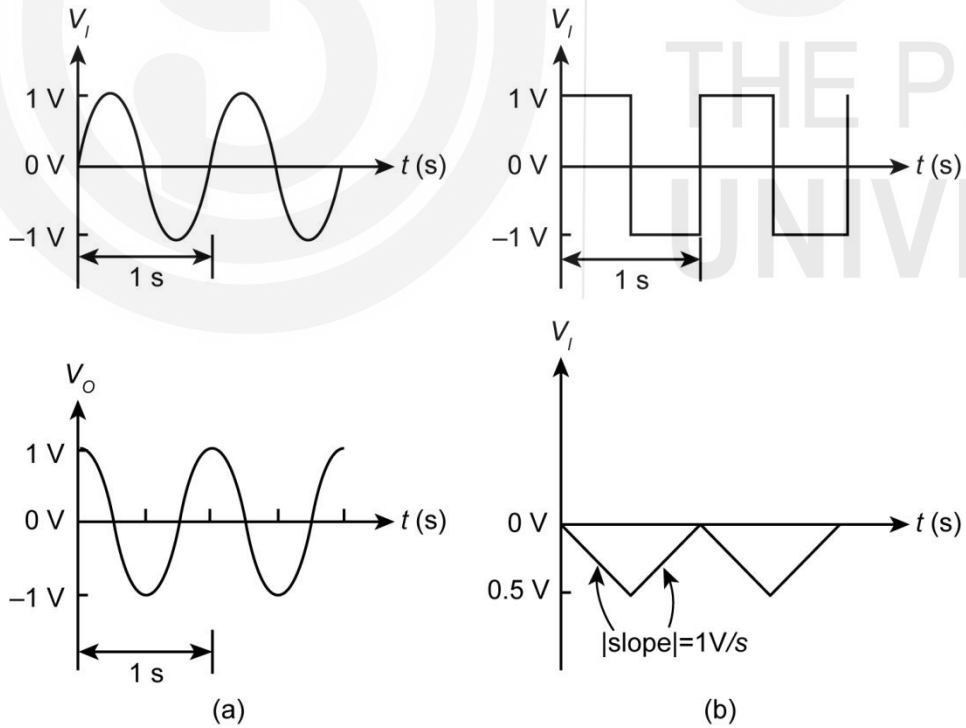


Fig. 14.19: **Output of a basic integrator when input is a) sine wave; b) square wave.**

In practical integrator circuit, a large value resistor R_F is connected in paralleled with C_F to provide a paralleled feedback path and avoid the charging of capacitor to V_{SAT} value. You will use this integrator circuit in the experiment you will perform in the laboratory course BPHEL-144.

Now attempt the following SAQ based on basic integrator.

SAQ 7 – Basic integrator

Trace the output waveform for the basic integrator shown in Fig. 14.20.

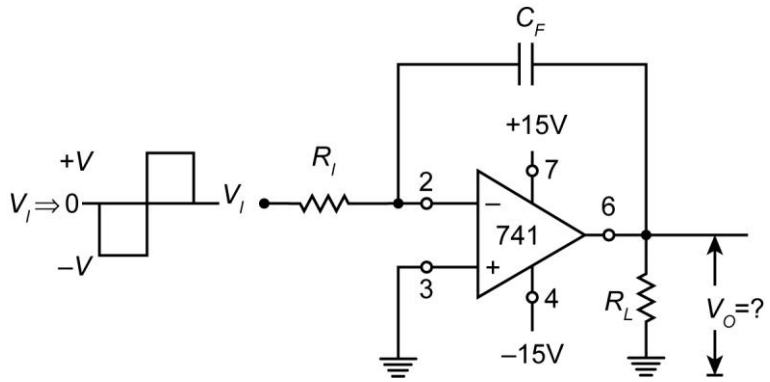


Fig. 14.20: **Output waveform of a basic integrator.**

Now we summarise the points discussed in this unit.

14.9 SUMMARY

Concept	Description
Comparator	■ Infinite open loop gain of an ideal op amp is used to obtain saturated voltage by comparing the inputs at non-inverting and inverting inputs. They can be used as voltage level detector.
Negative feedback in op amp	■ With the use of a feedback resistor R_F connecting pins 6 and 2, the closed loop gain of an op amp can be controlled.
Inverting amplifier	■ Inverting amplifier gain depends on the feedback resistor R_F and input resistor R_I. Negative sign in the equation for its gain means that there is a phase change of 180° between the input voltage and the output voltage. Input voltage is supplied to pin 2 in this case. This amplifier can be used as a multiplier or a divider.
Non-inverting amplifier	■ In non-inverting amplifier, there is no phase change between the input and output voltages. The input is given to the pin 3. The closed loop gain of this amplifier is always greater than unity.
Op amp adder	■ Inverting amplifier can have several inputs with common feedback resistor. Such a circuit can be used as an adder or to obtain average of input voltages.
Op amp subtractor	■ By using the op amp in differential mode, signal given to inverting input can be subtracted from the signal at non-inverting input.
Differentiator	■ In a basic differentiator, the input resistor is replaced by a capacitor. The output waveform of the differentiator is the derivative of the input waveform with opposite sign.
Integrator	■ In a basic integrator, the feedback resistor is replaced by a capacitor. The output waveform of the integrator is the integral of the input waveform with opposite sign.

14.10 TERMINAL QUESTIONS

1. Trace the output waveform of the circuit for the given input as shown in Fig. 14.21.

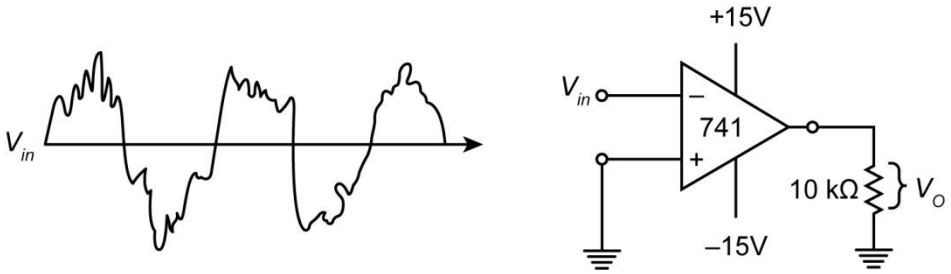


Fig. 14.21: **Irregular input to an inverting comparator.**

2. Design an amplifier using op amp 741C for a gain of –20 for an input of 0.5V and an output current of 5 mA.

3. Identify the circuit given in Fig. 14.22 and determine the value of output current. What changes should be made in the circuit so that output current is doubled without changing the gain of the amplifier?

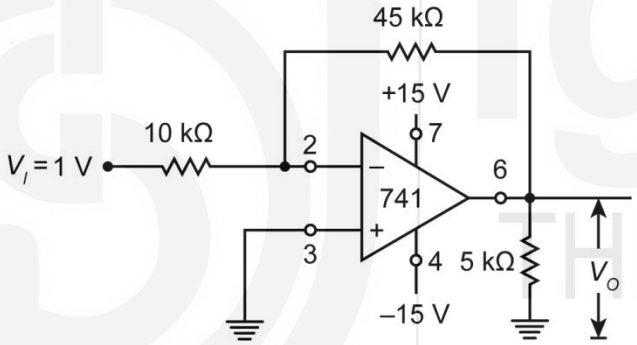


Fig. 14.22: **Op amp amplifier.**

4. Design an amplifier using op amp 741C for a gain +19. If the input voltage of 0.5V is to be amplified with an output current of 5 mA, determine the value of the load resistor.

5. If the inverting terminal (pin 2) is directly connected to output (pin 6) and input (V_{in}) is given to the non-inverting input terminal (pin 3), then what will be the output of the circuit?

6. Design a two-channel inverting adder with gains –8 and –17.

7. Design a differentiator circuit with its output twice the derivative of the input signal.

8. Design an integrator circuit the output of which is one-fifth the integral of the input signal.

14.11 SOLUTIONS AND ANSWERS

Self-Assessment Questions

1. The output waveform is shown in Fig. 14.23.

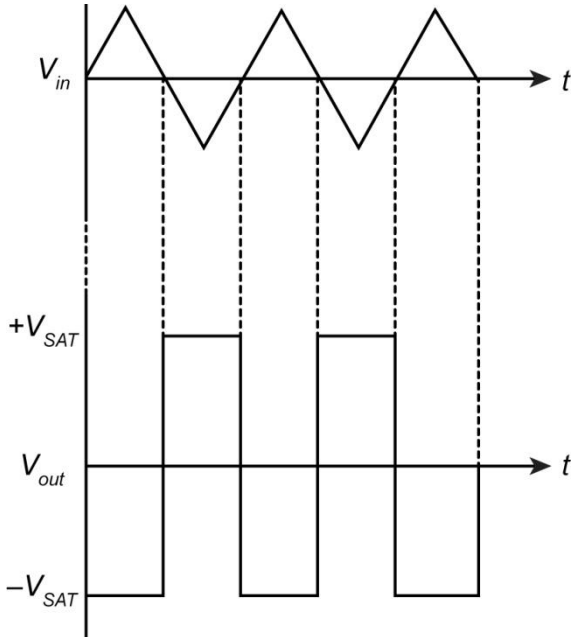


Fig. 14.23: **Op amp amplifier.**

2. If the feedback is connected to the non-inverting input, it will be in phase with the output voltage, i.e. it will act as positive feedback, and drive the output to saturation voltage.

3. The output voltage is $-V_{SAT}$, because the gain of the amplifier is –10. With +2V input, the output should be –20 V. However, the output cannot be greater than $+V_{SAT}$ and less than $-V_{SAT}$. Therefore the output is $-V_{SAT}$ which is approximately –13 V for the supply voltage of $\pm$ 15 V.

4. This is a non-inverting amplifier and its gain is $1+(R_F / R_I)$. With $R_F = 75\,\text{k}\Omega$ and $R_I = 15\,\text{k}\Omega$, the gain of the amplifier is 6.

5. The circuit is for an inverting adder. The output voltage is

$$V_O = -\frac{50\,\text{k}\Omega}{10\,\text{k}\Omega}(4-3+1)\,\text{V} = -5\times 2 = -10\,\text{V}$$

6. The output waveform is as given in Fig. 14.24.

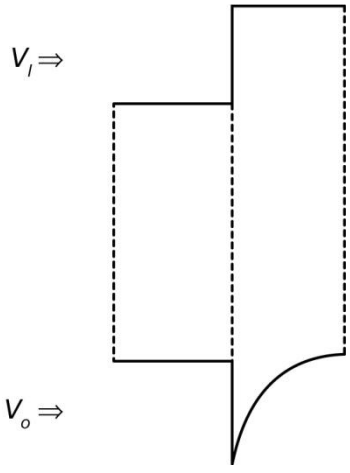


Fig. 14.24: **Output of a differentiator with input signal.**

7. The output waveform is as given in Fig. 14.25.

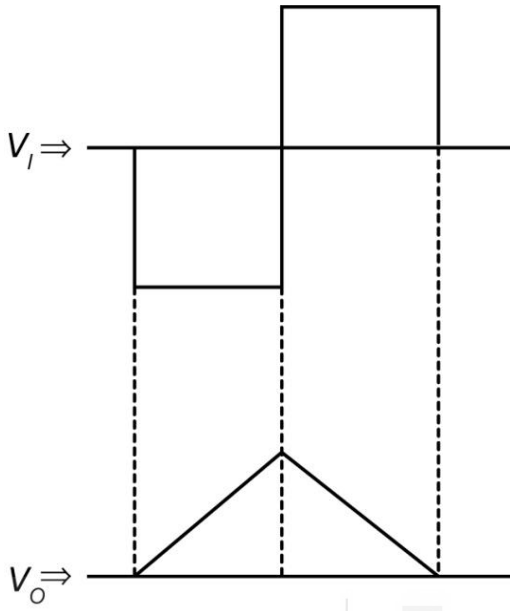


Fig. 14.25: **Output of an integrator with square wave input.**

Terminal Questions

1. The waveform is shown in Fig. 14.26.

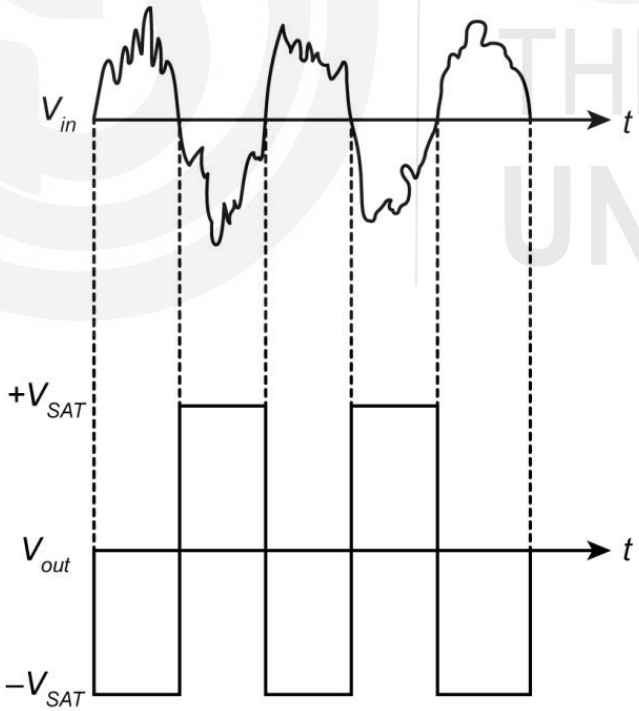


Fig. 14.26: **Output of a zero crossing detector.**

2. Choose the value of $R_I = 10\,\text{k}\Omega$. Therefore, for $A_{CL} = -20$,

$$R_F = |A_{CL}|R_I = 200\,\text{k}\Omega$$

We have,

$$I = 0.5\ \text{V}/10\ \text{k}\Omega = 0.05\ \text{mA}.$$

Now,

$$I_O = I + I_L$$

$$\therefore \quad 5\ \text{mA} = 0.05\ \text{mA} + I_L$$

$$I_L = (5 - 0.05)\ \text{mA} = 4.95\ \text{mA}$$

Now

$$A_{CL} = -20, \quad \therefore V_O = A_{CL} V_I = -20 \times 0.5\ \text{V} = -10\ \text{V}$$

$$I_L = V_O / R_L = 10\ \text{V}/R_L = 4.95\ \text{mA}.$$

$$\therefore \quad R_L = 10\ \text{V}/4.95\ \text{mA} = 2.02\ \text{k}\Omega.$$

Therefore, the components of inverting amplifier are
$R_I = 10\ \text{k}\Omega, R_F = 200\ \text{k}\Omega$ and $R_L = 2\ \text{k}\Omega$. Use $\pm$15V power supply.

3. The given circuit is of an inverting amplifier with gain = – 4.5. The output voltage is – 4.5 V.

   Now

$$I_O = I + I_L = \frac{1\ \text{V}}{10\ \text{k}\Omega} + \frac{4.5\ \text{V}}{5\ \text{k}\Omega}$$

$$= 0.1\ \text{mA} + 0.9\ \text{mA} = 1\ \text{mA}.$$

   For doubling the output current without changing the gain of the amplifier, I_L should be = 1.9mA.

   Therefore, $R_L = 4.5\ \text{V}/1.9\ \text{mA} = 2368\ \Omega$

   Thus, the value of R_L should be reduced from 5 kΩ to 2368 Ω.

4. The (+) sign with gain +19 means that we have to design a non-inverting amplifier. Its gain is $(1 + (R_F / R_I))$. It means that R_F / R_I should be 18. Choose $R_I = 10\ \text{k}\Omega$, then $R_F = 180\ \text{k}\Omega$. The output voltage is

$$V_O = 19 \times 0.5\ \text{V} = 9.5\ \text{V}.$$

   Now $I_O = I + I_L = 5\ \text{mA} = (0.5\ \text{V}/10\ \text{k}\Omega) + I_L$

   or $I_L = (5 - 0.05)\ \text{mA} = 4.95\ \text{mA}.$

   and $R_L = V_O I I_L = 9.5\ \text{V}/4.95\ \text{mA} = 1919\Omega$

Thus, the required design is $R_I = 10\,\text{k}\Omega, R_F = 180\,\text{k}\Omega$ and $R_L = 1919\,\Omega$ or $\approx 2\,\text{k}\Omega$.

5. The circuit of the configuration described in the question is shown in Fig. 14.27.

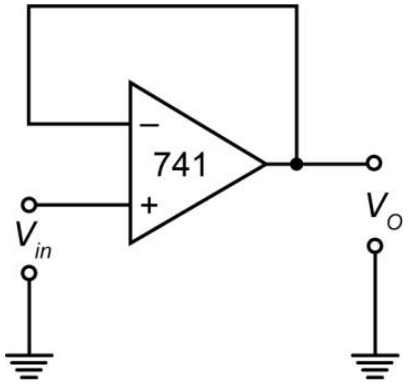


Fig. 14.27: **Unity gain amplifier.**

This circuit is a modified form of non-inverting amplifier, with $R_F = 0$ and $R_I = \infty$. Hence, with the gain formula for non-inverting amplifier, we get

$$A_{CL} = \left(1 + \frac{R_F}{R_I}\right) = \left(1 + \frac{0}{\infty}\right) = 1$$

Hence it is called a **unity gain amplifier**; or a **buffer amplifier**. The output of the circuit is exact replica of the input signal. However, due to the ability of op amp to source large output current, this circuit is used as a buffer circuit, that provides large input impedance to the input signal source and low output impedance for the load driven by it.

6. Choose $R_{I1} = 10\,\text{k}\Omega$ for channel-I with gain –17. Therefore, $R_F = 170\,\text{k}\Omega$ which is common to both the inputs. To find R_{I2} for the channel-2, we have

$$R_F / R_{I2} = -8$$

$$\therefore \quad R_{I2} = 170\,\text{k}\Omega/8 = 21.25\,\text{k}\Omega.$$

Thus the required design is $R_{I1} = 10\,\text{k}\Omega, R_{I2} = 21.25$ or $\approx 20\,\text{k}\Omega$. $R_F = 170\,\text{k}\Omega$ and choose $R_L = 5\,\text{k}\Omega$ (as no particular current requirement is stated).

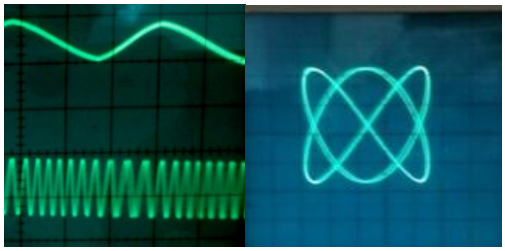
7. Basic differentiator output is

$$V_O = -R_F C_I \left(\frac{dv_I}{dt}\right)$$

Given is $R_F C_I = 2$. Choose $C_I = 1\mu\text{F}$ then $R_F = 2\,\text{M}\Omega$ so that $R_F \times C_I = 2$. Thus with $C_I = 1\mu\text{F}$ and $R_F = 2\,\text{M}\Omega$, the output will be twice the derivative of the input signal.

8. Basic integrator output is $V_O = -\frac{1}{R_I C_F}\int V_I \, dt$

For the output to be one-fifth of the integral of the input, $R_I C_F$ should be = 5. Therefore, choose $C_I = 1\mu F$ and $R_I = 5\,M\Omega$ so that $R_I C_F = 5$. Thus, with $R_I = 5\,M\Omega$ and $C_F = 1\mu F$, the output of the basic integrator will be one-fifth of the integral of the input signal.



Cathode ray oscilloscope is used to display the waveforms in various instruments used for scientific research, health monitors in medical treatment, radars used in aircraft traffic controls etc.

UNIT 15

CATHODE RAY OSCILLOSCOPE

Structure

STUDY GUIDE

In the first semester Mechanics: Laboratory course (BPHCL-132) you got an opportunity to use the cathode ray oscilloscope (CRO), while studying the Lissajous figures. You must have got conversant with the main functional knobs on the CRO at that time. In this unit we will be discussing in details the construction and working of a CRO. You will also get to know the different types of CROs used in the laboratories.

You will be able to understand the mechanism used for tracing the waveform on the CRO screen, if you revise your knowledge about electron deflection in electric field from your school physics courses. You can use the knowledge gained in this unit to operate the CRO in your laboratory more effectively.

"The oscilloscope provides the service technician with a "third eye" enabling him to see what is happening in the many electronic circuits with which he works."

Paul Smith

15.1 INTRODUCTION

A Cathode Ray Oscilloscope, abbreviated as CRO and referred to as oscilloscope, in short, is now a basic, important and versatile instrument in every electronics and electrical engineering laboratory. In your laboratory courses you have learnt that voltmeters are used to measure the voltage signals. If that voltage is dc, that is not varying with time, then we get accurate measurement. If the signal is a pure sine wave, then ac voltmeter can be used to determine its root mean square value. However, we cannot measure its frequency with even the ac voltmeter. If the signals are more complicated (like a square wave, which contains many harmonics of sinusoidal signals), no voltmeter can give the proper reading of the voltage. To display and study a signal or a waveform of any simple or complicated type, we use CRO.

On a CRO, you can measure important characteristic of a signal like ac or dc voltage, period, frequency, phase relationships, indirect measurement of ac or dc current and a wide range of waveform evaluations such as rise time, fall time, ringing, and overshoot. On a CRO screen, a luminous spot enables us to study the instantaneous value of input voltage. For this reason, an oscilloscope can also be viewed as a plotter or a recorder.

In this unit we will familiarize you with CRO and functions of its various control knobs in Sec. 15.2. In Sec. 15.3 you will learn about the construction and working of the main work-horse of the oscilloscope – the Cathode Ray Tube (CRT). You will also understand how the trace of a signal is generated on the CTR screen and obtain the expression for its deflection sensitivity.

In Sec. 15.4 we describe the different subsystems of a CRO. Although most common CRO can trace a single waveform there are many advanced types of CROs that can trace two or more signals at a time of the screen. In Sec. 15.5 you will learn about some special types of CRO used in the laboratories.

In Sec. 15.6 you will learn the important applications of CRO to trace the waveform, measure the peak amplitude of the signal, measure the period and obtain the frequency of the signal. You will also learn to find the difference in phases of two sinusoidal signals.

Expected Learning Outcomes

After studying this unit, you should be able to:

- describe the major subsystems of a CRO;
- explain the mechanism of obtaining the trace on the CRT;
- familiarize with various controls on the front panel of the CRO;
- explain the basic functions of various controls;
- draw the block diagram of a CRO;

- explain the construction and working of a cathode ray tube (CRT);
- define the deflection sensitivity of CRT and obtain its expression;
- describe different types of laboratory oscilloscopes;
- explain the method to measure the peak-to-peak voltage and frequency of a time varying waveform; and
- measure the phase difference between two sinusoidal waveforms.

15.2 FAMILIARIZATION WITH CATHODE RAY OSCILLOSCOPE (CRO)

The cathode ray oscilloscope is probably the most versatile electrical measuring instrument available. To observe various signal parameters listed in the introduction, the CRO has to be properly set. There are many control knobs on the front panel of the CRO. You should get familiarized with these controls in order to make proper use of the CRO.

For proper operation of an oscilloscope, all the controls are mounted on the front panel. Fig.15.1 depicts the location of various controls on the front panel of a typical general purpose dual trace oscilloscope. In such a CRO, two signals can be viewed simultaneously on two separate channels. We may add here that the location of different controls can vary from one model of CRO to another.

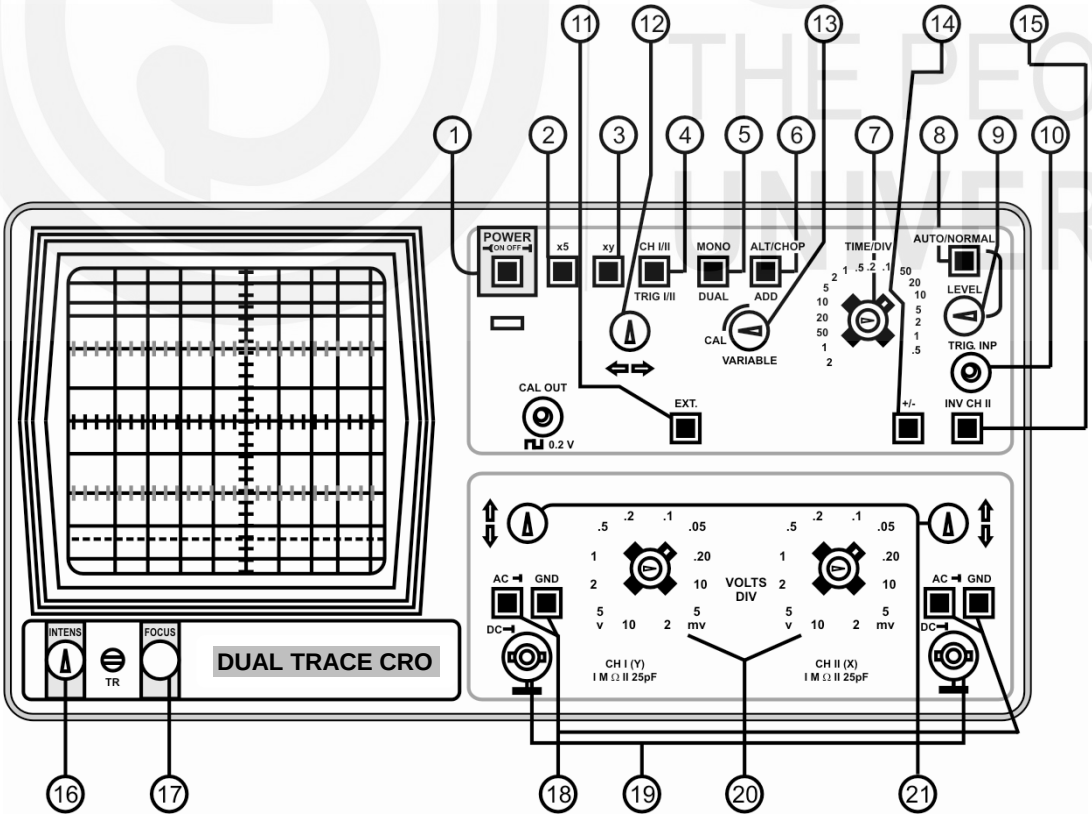


Fig.15.1: **Schematic diagram of front panel of a typical general purpose CRO.**

You must carefully read and understand the function of each control. Table 15.1 describes the function of each control shown in Fig. 15.1.

Table 15.1: Controls on CRO front panel

No.	CONTROL	FUNCTION
1.	Power	Turns mains power on/off.
2.	× 5	When pressed gives five times magnification of the signal.
3.	*X*-*Y*	It cuts off the time base fed to the horizontal plates when pressed and allows access to the horizontal signal fed through CH-II. It is used for *X*-*Y* display.
4.	CH-I/CH-II/Trig I/Trig II	It selects and triggers CH-I when it is out. On pressing it select and triggers CH-II.
5.	Mono/Dual	A switch to select the single/duel beam operation.
6.	Alt/Chop/Add	It selects alternate or chopped mode in DUAL trace operation. If "Add" is selected, it enables addition or subtraction of signals on two channels.
7.	Time/Div	It selects time base speeds.
8.	AUTO/NORM	AUTO mode enables trace when no signal is fed at the trigger input. In NORM position, the trigger level can be varied using LEVEL control.
9.	LEVEL	It allows setting of the trigger level between peak-to-peak amplitude of the input signal.
10.	TRIG IN	A socket that is used to feed external trigger signal in EXT mode.
11.	EXT	Switch that allows External triggering signal to be fed from the socket marked TRIG IN.
12.	*X*-POS	This knob controls the horizontal position of the beam trace.
13.	VAR	Controls the time base speed in between two steps of TIME/DIV switch.
14.	+/-	This switch selects the slope of triggering.
15.	INV CH.II	This switch when pressed inverts the signal at CH.II.
16.	INTENS	It controls the trace brightness.
17.	FOCUS	It controls the sharpness of the trace.
18.	DC/AC/GND	Coupling switch for each channel to choose AC or DC or ground.
19.	CH-I (*Y*) and CH-II (*X*)	BNC connectors serve as *Y*-input connections for CH-I and CH-II. CH-II input connector also serves as Horizontal external signal on using *X*-*Y* control.
20.	Volts/Div.	A switch to select the vertical sensitivity of each channel.
21.	*Y*-Pos I and II	These controls are provided for vertical deflection of trace for each channel.

SAQ 1 – Controls on the CRO front panel

Which control will you use if

a) the line being displayed on the screen is not sharp?

b) the amplitude of the signal being displayed goes beyond the height of the CRO screen?

c) you want to display two different signals simultaneously?

After getting familiarized with the functions of different controls of the CRO, we will now discuss about its construction and working.

The oscilloscope consists of the following major subsystems:

- Cathode ray tube or CRT
- Vertical amplifier
- Horizontal amplifier
- Sweep generator
- Trigger circuit
- Associated power supplies

The block diagram of a typical CRO is shown in Fig. 15.2.

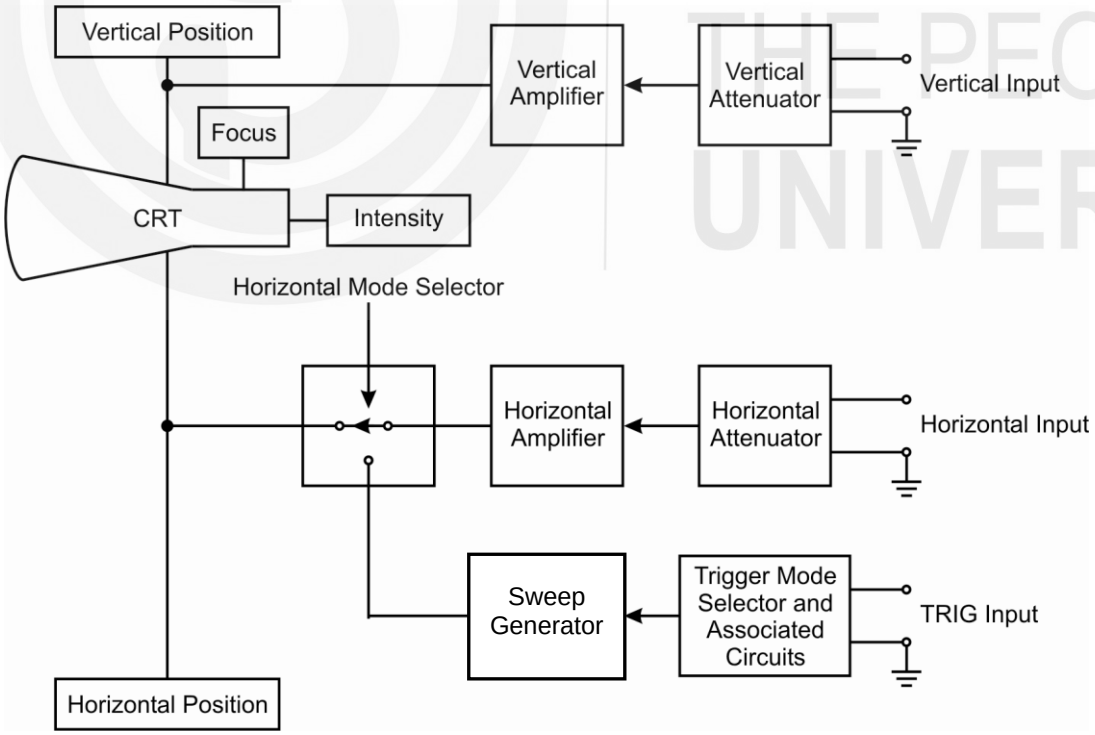


Fig.15.2: **Block diagram of a general purpose CRO.**

The heart of the instrument is the cathode ray tube. The remaining sub-systems are necessary for signal conditioning so that a visual representation of the input signal is done properly on the screen of the CRT.

15.3 CATHODE RAY TUBE (CRT)

The cathode ray tube used in an oscilloscope is very similar to the picture tube used in the old television sets. Let us first understand its components.

15.3.1 Construction of Cathode Ray Tube

A cross sectional representation of a CRT is shown in Fig. 15.3. The major components of a general purpose CRT are:

- Evacuated glass envelope
- Electron gun assembly
- Deflection plate assembly
- Phosphor coated fluorescent screen

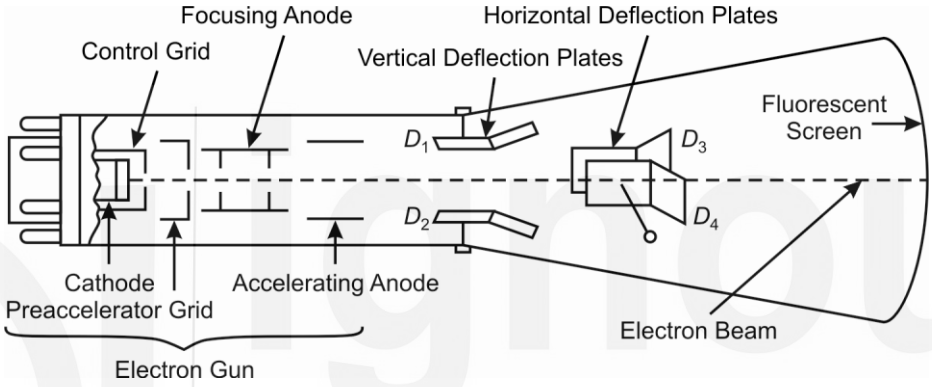


Fig. 15.3: **Schematic of a cathode ray tube showing its major components.**

The glass envelope is evacuated to a fairly high vacuum to permit the electron beam to traverse the tube easily. Most laboratory quality oscilloscopes use a CRT which has circular screen approximately 5 inch in diameter. All electrical connections except the high-voltage connection are made through the base of the CRT.

15.3.2 Generation of Electron Beam

The electron gun assembly consists of a heater to indirectly heat the cathode, a control grid, focussing anode and accelerating anode. The purpose of the electron gun assembly is to provide a source of electrons, converged and focussed into a well-defined beam, which is accelerated towards the fluorescent screen. The electrons that make up the beam are given off by thermionic emission from the heated cathode. The cathode is surrounded by a cylindrical cap that is at a negative potential. This acts as a control grid. Because the control grid is at negative potential, electrons are repelled away from the cylinder walls and, therefore, stream through the hole where they move into the electric field of the focussing and accelerating anodes. The magnitude of the accelerating field is given by

$$E = \frac{V_a}{d} \qquad (15.1)$$

where, V_a is the accelerating anode voltage and d is the distance between the cathode and second anode measured in meters. When electrons enter the

electric field, which is assumed to be of uniform intensity, a force will be exerted on the electrons that will accelerate them along the axis of the tube. The magnitude of the force is given by

$$F = Eq = ma$$

$$\therefore \quad a = \frac{Eq}{m} \qquad (15.2)$$

where a is the acceleration produced due to the electric field. E is electric field intensity, q is electronic charge = 1.6×10^{-19}C and m is the mass of electron $= 9.1 \times 10^{-31}$kg. Using the expression for electric field from Eq. (15.1) in Eq. (15.2) we obtain

$$a = \frac{V_a q}{dm} \qquad (15.3)$$

During the period of acceleration, the electrons gain kinetic energy as they gain velocity. If v is the velocity acquired then,

$$\frac{1}{2}mv^2 = Fd = V_a q$$

which implies that,

$$v = \sqrt{\frac{2V_a q}{m}} \qquad (15.4)$$

15.3.3 Deflection of Electrons in CRT

After the electrons leave the electron gun assembly at a speed given by Eq. (15.4), they enter and pass through a region controlled by the deflection plates. One pair of plates controls the vertical motion of the beam while the other pair controls the longitudinal components of the electron velocity. The deflection plates are described by two geometric parameters, the length (L) of the plates and the plate separation (s). The deflection action of the plates depends on the intensity of the electric field (E_d) between the deflection plates given by

$$E_d = \frac{V_d}{s}$$

where V_d is the magnitude of the deflecting voltage. This field will exert a force $F_d = E_d q$ on the electrons, deviating the beam from a straight line trajectory.

$$F_d = E_d q = \frac{V_d}{s} q = ma_y$$

$$\Rightarrow \quad \text{Acceleration along } y\text{-axis, } a_y = \frac{V_d q}{ms} \qquad (15.5)$$

It can be shown (refer to the margin remark) that the vertical distance travelled by electron is given by

$$h = \frac{V_d q t^2}{2sm} \qquad (15.6)$$

where t is the time required for electron to pass through the plates, given by

$$t = \frac{L}{v}$$

We use the identity: distance travelled in time t,

$$x = \frac{1}{2}at^2$$

where a is the acceleration.

Here v is the velocity of electron when it comes out of electron gun assembly given by Eq. (15.4) and L is the length of the deflection plate.

Combining Eqs. (15.6) and (15.4), we get

$$h = \frac{L^2 V_d}{4 V_a s} \tag{15.7}$$

Fig. 15.4 shows the deflection geometry of the CRT.

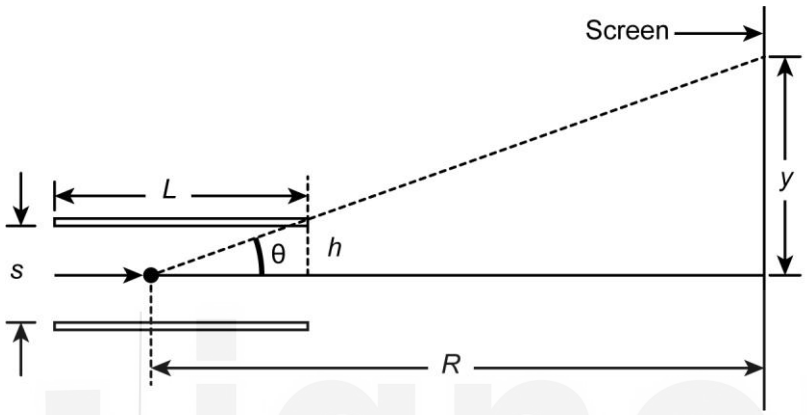


Fig. 15.4: **Deflection of electron beam in CRT.**

Using small angle approximation ($\sin\theta \approx \theta$) from Fig. 15.4 we can write,

$$\theta = \frac{h}{L/2} = \frac{2h}{L} = \frac{y}{R}$$

$$\Rightarrow \quad y = \frac{2hR}{L}$$

$$= \frac{RLV_d}{2V_a s}$$

$$\Rightarrow \quad \frac{V_d}{y} = \frac{2V_a s}{RL} \tag{15.8}$$

The term $\frac{V_d}{y}$ is referred to as **deflection sensitivity** and is defined as voltage required per unit deflection.

The deflection of the beam in CRT is obtained electrostatically. You should note that the potential applied across the horizontal plates D_1 and D_2 in Fig. 15.3 would deflect the beam vertically, whereas a potential applied to vertical plates D_3 and D_4 would deflect the beam horizontally. Further, you learnt that the magnitude of the deflection is proportional to the voltage applied across the horizontal/vertical plates. In a CRT, with display screen of about 10 cm, under ordinary conditions, a deflection of about 2.5 cm could be obtained for a potential of about 100V. Since the signals are well below 100V in a real situation, we need to amplify signals. Therefore, deflection amplifiers are provided for each pair of deflection plates.

When the electron beam strikes the phosphor-coated face of the CRT, a spot of light is produced due to "fluorescence" as phosphor is a florescent material such as ZnS. The high velocity electrons that strike the phosphor coated face of the CRT are either repelled by the collision or cause secondary emission of electrons to maintain electrical equilibrium of the screen. To provide return path to ground for these electrons, the inside surface of the CRT is coated with graphite called "aquadag".

To understand the relationship between the applied deflection potential and resultant deflection of the beam, solve the following SAQ.

SAQ 2 – Deflection of beam in CRT

In a CRT, the separation between the deflection plates is 6 mm, length of the plates is 3 cm, distance between the screen and the centre point of the deflection plates is 10 cm. If accelerating potential applied to anode is 1000V, the beam is deflected by 2 cm on the screen. What is the applied deflection voltage? Calculate the deflection sensitivity of the CRT.

15.3.4 Obtaining a Trace on the CRT Screen

You may now like to understand, how a waveform is displayed on the CRO screen. Refer again to Fig. 15.4. For a dc-voltage applied to plates D_3 and D_4 (horizontal deflection plates), the spot on CRO screen will move either to the left or to the right, depending on whether D_3 is at a lower or higher potential than D_4. In order to generate a straight line on CRO display screen, a linearly increasing voltage with time (called ramp waveform) is applied between D_3 and D_4. This shifts the spot from extreme left to extreme right of the screen. If the voltage is brought to zero and again applied, the motion of electron beam (spot on the screen) may be repeated from left to right. Such a waveform is called a saw-tooth waveform, as shown in Fig. 15.5. If this process is repeated at a faster rate, you will see a straight line formed by the moving spot due to persistence of vision. An oscillator which generates such a voltage is called a saw-tooth oscillator or a sweep generator.

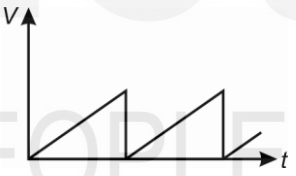


Fig. 15.5: **Saw-tooth Waveform.**

When a dc-voltage is applied to plates D_1 and D_2 (vertical deflection plates), you may see the spot moving up or down on the screen depending on the potential of D_1 relative to D_2. If we apply a time varying waveform like sinusoidal, square, triangular etc. across the vertical deflection plates, it will also appear as a spot moving up and down on the screen. However, application of a saw-tooth waveform to the horizontal deflection plates gives rise to display along the time axis. Let us now understand how display evolves on time scale.

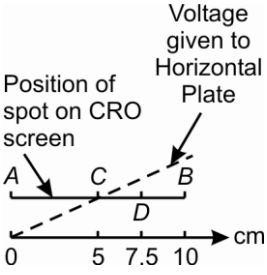


Fig. 15.6: **Horizontal time base of CRO.**

The time period of a saw-tooth wave of frequency 50 Hz, applied to the horizontal deflection plate (Fig. 15.5) is 20 ms. Suppose that it traces a line of length AB = 10 cm on CRO screen, as shown in Fig. 15.6. Then at t = 0, the spot will be located at the point A. After 10 ms, it will be at the point C as the saw-tooth voltage increases to half of its peak value. After 15 ms, the spot will reach the point D such that AD is three fourth of the line AB. In this way, you

can calibrate line *AB* in time, i.e., half of it to 10 ms; quarter of it to 5 ms and so on.

Consider that a sinusoidal signal of frequency 50 Hz shown in Fig. 15.7a is applied to vertical deflection plates. At the same time we apply internally generated saw-tooth voltage of the same frequency across the horizontal deflection plates (Fig. 15.7c). The trace obtained on the CRO screen is shown in Fig.15.7b. Note that at A_1, the sinusoidal wave has zero voltage and so there will be no deflection in the vertical direction. The horizontal input corresponds to the lowest voltage at A_1' and thus the spot moves to the extreme left point *A* on the screen. After 5 ms, the vertical input will correspond to A_2. This will move the spot upward. Since at the same time the horizontal input is less negative at A_2', the spot moves rightwards as well. This results in the position *B* of the spot on the CRO screen. After 10 ms, the vertical and the horizontal inputs will correspond to points A_3 and A_3', respectively; the voltage will be zero. This leads the spot to move to point *C* on the screen. Continuing in the same way, we finally obtain the points *A*, *B*, *C*, *D* and *E* on the CRO screen corresponding to points A_1, A_2, A_3, A_4 and A_5 on the vertical input and A_1', A_2', A_3', A_4' and A_5' on the horizontal input.

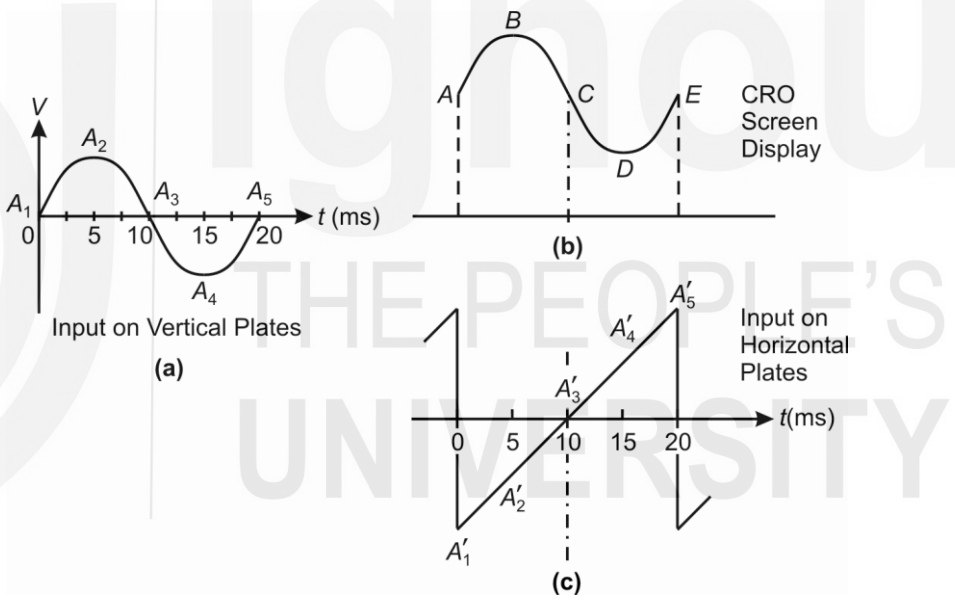


Fig. 15.7: **Display of 50 Hz sinusoidal wave on CRO: a) input to vertical deflection plates; b) trace on the CRO screen; c) input on the horizontal deflection plates.**

From the above discussion, you can conclude that for **an oscilloscope to display the variation of an electrical signal in the vertical direction as a function of time, a voltage varying linearly with time such as a saw-tooth wave will have to be applied on the horizontal deflection plates. The frequency of internally generated saw-tooth waveform can be selected by using the time base (time/div) control.**

To provide a stable trace, an additional feature in the form of a *trigger* is provided in the oscilloscopes. While using a trigger, the CRO pauses in each cycle when the sweep reaches extreme right side of the screen and retraces back to the left hand side of the screen. Then it waits for a specified event before starting the next trace. The trigger event is usually the input waveform

reaching some user-specified threshold voltage in a specified direction (going positive or negative).

Before proceeding further, solve an SAQ.

SAQ 3 – Choice of time base

If you wish to display a single cycle of 1 kHz sine wave signal on the entire 10cm width of CRO screen, plot the saw-tooth waveform given to the horizontal deflection plates (similar to Fig. 15.7c) with proper scale on the time axis.

After getting acquainted with working of a typical CRO, we will now discuss about the types of CRO commonly used in the laboratories.

15.4 LABORATORY OSCILLOSCOPES

15.4.1 Dual Trace Oscilloscope

A dual trace is obtained by electronically switching the single electron beam between two channels. Fig. 15.8 shows a block diagram of the two vertical input channels and the electronic switch that alternately connects the two input channels to the vertical amplifier. There are generally at least four modes of operation with dual trace oscilloscopes; they are labelled A, B, alternate (ALT), and chopped (CHOP). When set to A or B, only the input of that channel is displayed. In the alternate mode the inputs are displayed on alternate traces. Since the switching rate is synchronised with the sweep generator, switching occurs at the same rate as the output of the sweep generator. The “alternate mode” of operation is generally preferred when displaying relatively high-frequency signals.

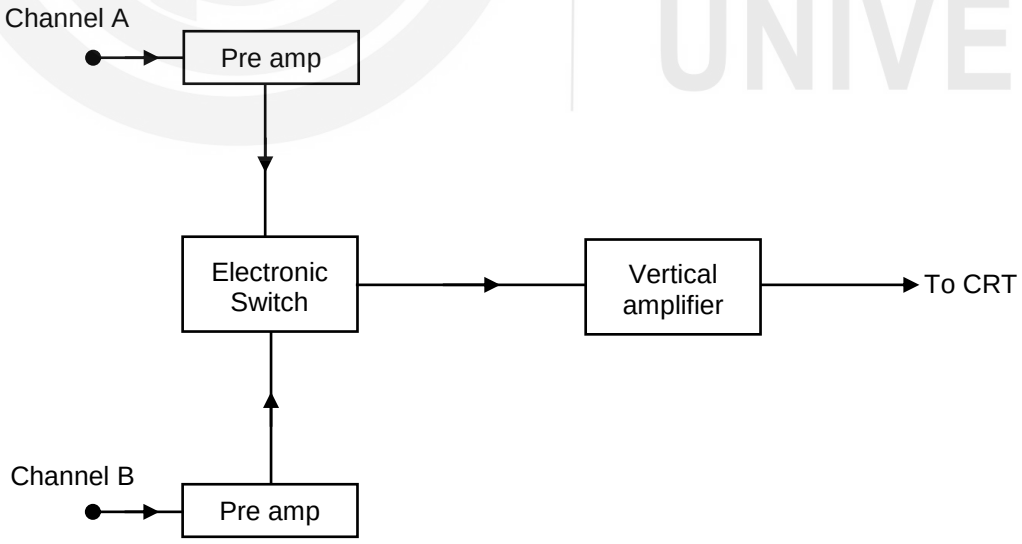


Fig. 15.8: **Block diagram of the input channels of a dual trace oscilloscope.**

In the “chopped mode”, electronic switching occurs at a rate completely independent of the sweep rate, and therefore, each display has portions missing during which time the other signal is being displayed. The chopped mode is normally used at low sweep rates when the alternate mode would provide a display with appreciable flicker.

15.4.2 Storage Oscilloscope

There are many oscilloscope applications where the limited persistence of the CRT phosphor makes real time observation of one-time events nearly impossible. Although such events can be recorded photographically, this may prove to be fairly expensive and time consuming. The storage oscilloscope makes it possible to retain a CRT display for an extended period of time. The storage CRT uses two electron guns – the usual electron gun called a writing gun and a flood gun which uniformly bombards the entire CRT screen with low-energy electrons.

The storage is achieved due to secondary emission phenomenon. When the writing gun bombards electrons on the phosphor screen, alongwith causing a short duration illumination of the phosphor, the kinetic energy of the electrons knocks out some electrons from the screen, where the beam strikes. So this region of the screen has some net positive charge, in comparison with the other parts of the screen, where writing beam has not fallen.

Now, the low energy electrons coming from the flood gun are supposed to be uniformly covering the entire screen area. But, due to net positive charge left on the trace area of the screen by the writing gun, these low energy electrons get strongly attracted to this region, illuminating it further.

By properly tuning the energy of the flood gun electrons, it is possible to make every low energy electron falling on the positively charged region to eject one secondary electron. So this preserves the positive charge on the illuminated area, and the next low energy electron from the flood gun can keep the illumination process going on in the similar way for a longer time. Finally, the screen is erased by grounding the phosphor screen, which removes the excess charge.

15.4.3 Digital Oscilloscope

The storage oscilloscopes described above are quite expensive and are now being replaced by digital oscilloscopes. In these oscilloscopes the signal being displayed is sampled and digitized. The amplitude and time base per cm are displayed in numbers at a corner of the screen. The digitized signal can be stored in a memory (like computer memory) and recalled (with the help of a digital-to-analog converter-DAC) to display whenever required. Thus, they also serve as storage oscilloscope.

SAQ 4 – **Dual trace CRO**

Which mode of dual trace oscilloscope is preferred at high frequencies? Why?

Now we will explain the procedures to measure various signal parameters using a CRO.

15.5 APPLICATIONS OF CRO

The range of applications of oscilloscope varies from basic voltage, time, frequency measurements and waveform observations to highly specialised applications in all areas of science, engineering and technology.

We now describe some basic measurements carried out with a CRO.

15.5.1 Measurement of Peak Voltage

You can use an oscilloscope to measure both dc and ac voltage. To measure dc voltage, you should first keep the DC/AC/GND switch in the ground (GND) position to establish the ground (0 V) level on the screen. Next you change the DC/AC/GND selector switch to DC position to measure the dc voltage level. When the dc voltage to be measured is applied to the channel input using the probes of the CRO, the horizontal trace line shifts in vertical direction. This deflection of the trace can be used to measure the dc voltage by using the relation

dc voltage = vertical deflection of the trace (cm) × vertical sensitivity (V/cm)

To measure ac voltage, the DC/AC/GND switch is kept in the AC mode. On the screen the waveform corresponding to the input signal is observed. Now we measure the vertical distance between the maximum and minimum levels of the signal using the graduated scale on the screen, as shown in Fig. 15.9.

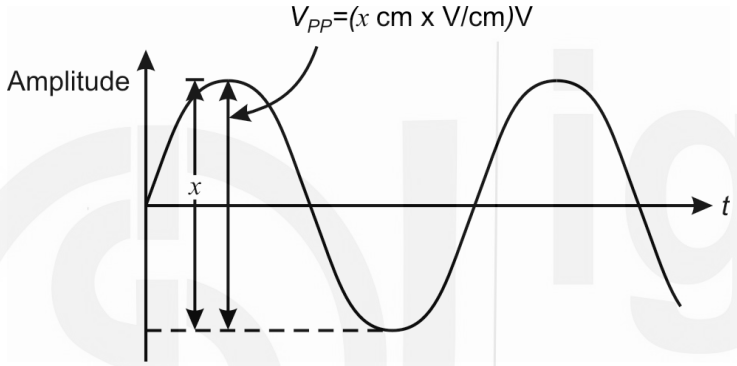


Fig. 15.9: **Peak-to-peak voltage measurement for ac-signal using CRO.**

By multiplying this distance (in cm) with the selected sensitivity (V/cm), we get the magnitude of peak-to-peak amplitude of the applied ac voltage (V_{PP}). You can calculate the root mean square (rms) value of the voltage by dividing V_{PP} by $\sqrt{2}$.

This can be easily explained with the following Example.

EXAMPLE 15.1: VOLTAGE MEASUREMENT USING CRO

For the waveform shown in Fig. 15.9, the peak of the trace is at 1.5 cm on the oscilloscope screen. If the vertical sensitivity is set to 0.5 volts/div, find the peak-to-peak and rms amplitude of the signal.

SOLUTION ■

$$V_{PP} = \frac{\text{volts}}{\text{div}} \times \text{no. of div}$$

The peak-to-peak amplitude of the signal is 2 times the height of the maximum.

Hence, $$V_{PP} = \frac{0.5\ \text{V}}{\text{div}} \times 3\ \text{div}$$

$$= 1.5\ \text{V}$$

$$V_{rms} = \frac{1.5\ \text{V}}{\sqrt{2}} = 1.06\ \text{V}$$

We now discuss how CRO can be used to measure frequency of an input signal obtained from an oscillator or a function generator.

15.5.2 Measurement of Frequency

To measure an unknown frequency, we have to essentially measure the period of the signal on the CRO screen. The period of the signal is the length of one cycle of signal on time (horizontal) axis in cm multiplied by the (time/div) setting. The frequency is given by the inverse of the period.

EXAMPLE 15.2: FREQUENCY MEASUREMENT USING CRO

Determine the frequency of the signal displayed on the CRO screen as shown in Fig.15.10.

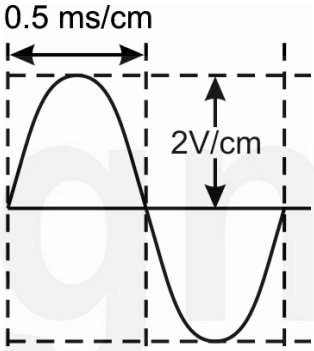


Fig. 15.10: **Frequency of trace displayed on CRO screen.**

SOLUTION ■

$$\text{Period} = \frac{\text{time}}{\text{div}} \times \text{no. of div}$$

The selected time/div is 0.5 ms/cm. One cycle of waveform is displayed over 2 divisions on the CRO screen.

Hence, $$\text{Period} = \frac{0.5\,\text{ms}}{\text{div}} \times 2\,\text{div} = 1\text{ms}$$

$$\text{Frequncy} = \frac{1}{\text{Period}}$$

$$= \frac{1}{1\text{ms}} = 1\text{kHz}$$

15.5.3 Measurement of Phase Difference

We can use an oscilloscope to determine the phase difference between two signals of same frequency by two methods:

- Direct measurement by comparing the two waveforms displayed simultaneously using a dual trace CRO; and
- Lissajous pattern method.

The first method is quite simple, and we will explain it now. You have already learnt (and used) the second method while doing the experiment on Lissajous Patterns in the first semester laboratory course entitled Mechanics: Laboratory (BPHCL-132).

Dual Trace Method

This method of determining phase difference between two waveforms of same frequency and equal or different amplitudes is quite accurate. It involves displaying both the signals on the CRO screen simultaneously. The distances (in time scale divisions) between two identical points on two traces (Fig.15.11) are measured. Here we choose one signal as a reference, that is, with zero-phase angle. Therefore, the signal being compared is said to be leading by an angle θ if it is to the left of the reference signal and lagging if it is to the right of the reference signal. The lead indicates positive value of phase while lag indicates negative value of phase.

To begin with, we obtain traces of both waveforms on the CRO screen, as shown in Fig. 15.11. For setting both patterns in the vertical centre of the display screen use AC switch.

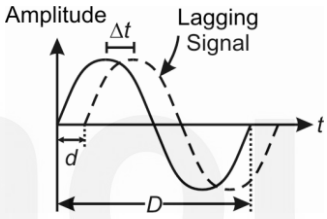


Fig.15.11: **Phase difference measured on dual trace CRO.**

Then we calculate the scale factor that correlates the distance on the CRO time axis (horizontal axis) with the phase angle in degree. For this we measure the horizontal distance D (cm) required for one full cycle of either waveform and calculate the scale factor (S) by using the relation

$$S = 360°/D \qquad (15.9)$$

Next, we measure the horizontal distance d (cm) between corresponding positive slopes of the two waveforms. The phase angle θ between the two waveforms is therefore obtained by:

$$\theta = S.\, d = \left(\frac{d}{D}\right) 360^\circ \qquad (15.10)$$

For these measurements, you may select the mode of operation-ALT or CHOP depending on the frequency of the signals. If the frequency of the input signal is less than 50 kHz, use CHOP mode. ALT mode is selected for frequencies greater than 50 kHz.

SAQ 5 – Phase difference between waves

In Fig. 15.11, if D = 6 cm and d = 3 mm, calculate the phase difference between the waves.

Now, we will summarize the points discussed in this unit.

15.6 SUMMARY

CONCEPT	DESCRIPTION
Cathode ray oscilloscope	■ Cathode ray oscilloscope comprises a cathode ray tube and allied electronic subsystems. On the screen of CRT waveform of input signal is displayed.

Time base

- Saw-tooth generator provides the horizontal sweep. Frequency of sweep generator sets the time/div (time base) scale.

Types of CRO

- Laboratory oscilloscope can be classified into three categories: i) Dual trace oscilloscope, ii) Storage oscilloscope; iii) Digital oscilloscope.

Applications

- Cathode ray oscilloscope is used for measurement of electrical parameters like, ac and dc voltage, time-phase relationship, frequency and for observing the shapes of various waveforms.

15.7 TERMINAL QUESTIONS

1. Explain the functions of main subsystems of a general purpose CRO.
2. Explain the two modes of operation of a dual trace CRO.
3. If the time/div control is set to 2 μs/div and a single cycle of displayed signal covers 4 div on the horizontal scale of the CRT screen, determine the frequency of the signal.
4. Determine the peak-to-peak amplitude and frequency of the signal shown in Fig. 15.12. The screen width is 10 cm and height is 8 cm. The voltage sensitivity is 2 V/cm and time base is 2ms/cm.

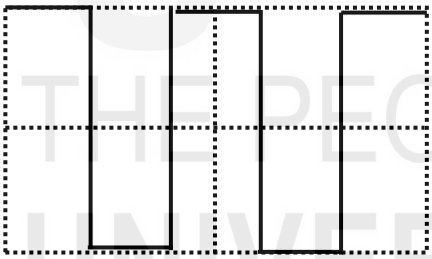


Fig. 15.12: **Signal trace on a CRO screen.**

15.8 SOLTUIONS AND ANSWERS

Self-Assessment Questions

1. a) Focus b) Volts / Div c) Mono / Dual
2. We use Eq. (15.8). It is given that

$$V_a = 1000\ \text{V},\ s = 6\ \text{mm} = 0.6\ \text{cm}$$

$$R = 10\ \text{cm},\ L = 3\ \text{cm},\quad y = 2\ \text{cm}$$

$$\therefore \quad V_d = \frac{2V_a\, s\, y}{R\, L}$$

$$= \frac{2 \times 1000\ \text{V} \times 0.6\ \text{cm} \times 2\ \text{cm}}{10\ \text{cm} \times 3\ \text{cm}} = \frac{2400\ \text{V cm}^2}{30\ \text{cm}^2} = 80\ \text{V}$$

$$\text{Deflection sensitivity} = \frac{V_d}{y} = \frac{80\ \text{V}}{2\ \text{cm}} = 40\ \text{V cm}^{-1}$$

3. The saw-tooth waveform given to horizontal deflection plates is shown in Fig. 15.13.

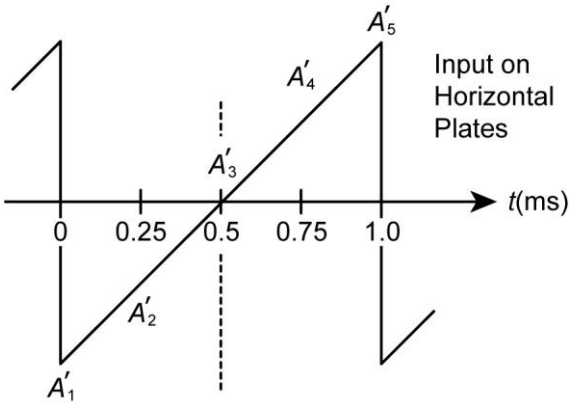


Fig. 15.13: **Saw-tooth waveform for 1 kHz signal.**

4. At high frequencies, the "alternate mode" of dual trace CRO is used. Since the sweep rates are higher, even when the two traces are traced alternately, due to persistence of vision of our eyes, both the channels can be seen simultaneously without any disturbance.

5. D = 6 cm, d = 3 mm = 0.3 cm

Using Eq. (15.10), the phase difference is

$$\theta = \left(\frac{0.3}{6}\right)360° = 18°$$

Terminal Questions

1. The main subsystems of oscilloscope and their functions are as follows:

- **Cathode ray tube or CRT** – generates a beam of electrons and display the input waveform on the screen after necessary deflections.
- **Vertical amplifier** – amplifies the input signal to be given to vertical deflection plates to an adequate level so that the beam can be deflected in vertical direction (representing the amplitude of the signal).
- **Horizontal amplifier** – amplifies the signal from the sweep generator to be provided to the horizontal deflection plates.
- **Sweep generator** – provides the saw-tooth waveform of selected frequency (by time/div time base control) to the horizontal deflection plates.
- **Trigger circuit** – provides the starting signal for every horizontal sweep.

2. Refer to Sec.15.4.1.

3. $$T = \frac{2\mu s}{\text{div}} \times \frac{4\ \text{div}}{\text{cycle}} = \frac{8\mu s}{\text{cycle}}$$

$$\therefore \quad f = \frac{1}{T} = \frac{1}{8\mu s} = 125\ \text{kHz}$$

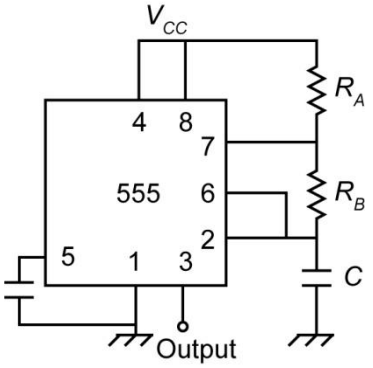
4. The amplitude of the waveform is covering entire 8 cm height of the screen. The sensitivity on vertical scale is 2 V/cm. Hence peak-to-peak amplitude of the signal is

$$V_{PP} = (2 \text{ V/cm}) \times 8 \text{ cm} = 16 \text{ V}.$$

The screen width is 10 cm. In this length, there are 2.5 cycles of the signal. Hence each cycle covers 4 cm length on the time axis. The selected time base is 2 ms/cm.

Hence, Period of the signal = (2 ms/cm) x 4 cm = 8 ms.

$$\text{Frequency} = \frac{1}{\text{Period}} = \frac{1}{8\,\text{ms}} = 125\,\text{Hz}.$$



Astable multivibrator using Timer IC555 is commonly used to generate clock signals as you will learn in this unit.

UNIT 16

TIMER CIRCUITS

Structure

STUDY GUIDE

The IC technology has allowed us to assemble many circuits together on single silicon chip and form a functional circuit. In this unit you will learn about the timer ICs, particularly IC555 timer.

To understand the working of IC555 you should brush up your knowledge about the operational amplifier as a comparator. Since the timing of these circuits are determined by charging-discharging times of a capacitor, you should refresh your knowledge about *RC* circuit from Experiment 3 in the Course on Electricity and Magnetism: Laboratory (BPHCL-134).

"The only reason for time is so that everything doesn't happen at once."

Albert Einstein

16.1 INTRODUCTION

In many application we require certain device to be on or off for a fixed length of time. For example, a valve of certain container should be open every 1 minute for only 3 seconds, and this process should continue till we switch off the system. Or we need a fire alarm that beeps every 2 seconds till corrective action is taken. All these applications require a system that generates electrical pulse signals at pre-determined time intervals and of pre-set width. Such signals are generated using the **timer circuits**. Most common of these circuits is a family of special circuits called **multivibrators**.

The name multivibrator is derived from the number of stable states that its output terminal has. Such circuits are useful in analog as well as that digital electronics. There are three categories of multivibrator circuits – astable, monostable and bi-stable. An **astable multivibrator** has no stable state at its output. Once it is powered, the output state keeps alternating between logical 0 and 1 continuously. Hence an astable multivibrator is essentially a rectangular wave oscillator. A **monostable multivibrator** can have either 0 or 1 (normally low or high) stable output state. When it receives a momentary trigger, the circuit makes a transition from its stable (quiescent) state to the other state. It stays in that state for a predetermined time period and then on its own, returns to the quiescent state. A **bi-stable multivibrator** can have two output states. Like the monostable multivibrator, it also changes its output state in response to a suitable triggering pulse but it does not return to the previous state on its own. To bring it back to the previous state, another pulse must be externally provided.

All three categories might produce repetitive rectangular waveform if they are suitably operated or triggered. The rectangular (or square) waveform is predominant in today's world of digital electronics, electronic communication and computers. Although initially all multivibrators were constructed using discrete devices such as transistors, they were later integrated on semiconductor chips (ICs).

The multivibrators can be built by using a popular analog integrated circuit called **Timer IC** and its identifying number is **IC555**.

In this unit we will introduce you to IC555. Its basic information and details of working along with block diagram are given in Sec. 16.2. The main two modes of operating timer IC555 are astable mode and monostable mode.

In certain applications, we require a single pulse to be generated in response to some trigger, like switching off the valve for a set period of few minutes when the tank is full or keep an indicator LED on for same seconds when a process gets over. In all such situations we need a single pulse starting with same control signal (trigger). A circuit producing such single pulse is called a **monostable multivibrator** or a **mono-shot**. In Sec. 16.3, you will learn about the circuit and working of monostable operation of IC555. You will also learn to design a monostable multivibrator having desired pulse width.

In **astable multivibrator** or **free-running mode**, a continuous pulse train of desired duty cycle is generated. These pulses can be used as clock pulses for

any control circuit or can drive an LED which keeps on continuously blinking (switching on and off) depending on the *ON*-time and *OFF*-time of the pulses. You will learn about the circuit diagram and operation of astable multivibrator in Sec. 16.4. You will also learn to design an astable multivibrator of desired frequency with requisite duty cycle.

You will get an opportunity to design and build both these multivibrators in the laboratory course BPHEL-144 entitled Digital and Analog Circuits and Instrumentation: Laboratory. So we suggest that you should learn this unit very carefully.

Expected Learning Outcomes

After learning this unit, you should be able to:

- identify the different pins of IC555 and understand their functions;
- draw a block diagram of IC555 and explain its working;
- write the applications of IC555;
- explain the working of monostable multivibrator using IC555;
- design a monostable multivibrator of required pulse width using IC555;
- draw the circuit diagram of astable multivibrator using IC555 and explain its working; and
- design an astable multivibrator of given frequency and duty cycle using IC555.

16.2 IC555 FUNDAMENTALS

IC555 is a landmark IC introduced by Signetics Corporation in 1971. This more than 50 year old IC has been a main component of many electronic circuits due to its versatile nature. It can provide output in rectangular waveform or as analog waveforms representing charging-discharging of a capacitor. The rectangular wave output can take either high or low state, so it is very appropriate to be used with digital circuits also. This versatility makes it one of the most popular analog IC.

Now let us give you some of its basic information.

16.2.1 Basic Information of IC555

IC555 is an 8-pin IC with pin-out diagram as shown in Fig. 16.1.

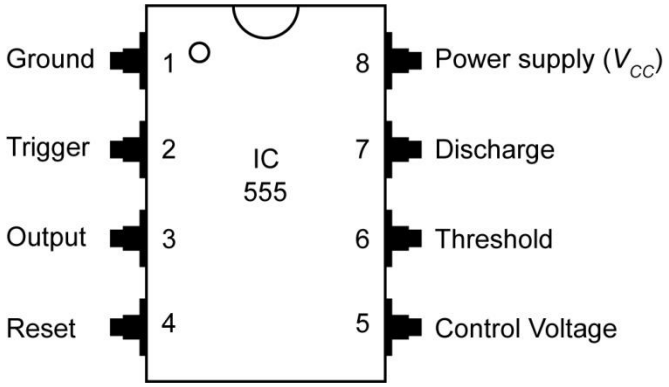


Fig. 16.1: **Pin-out diagram of IC555**.

This IC can work with a single polarity supply ranging over a wide range from +4.5 to +18 V. By using a +5V supply, the circuit can be made directly compatible with the digital circuits, means its output voltage levels are 0 V and 5 V, which can be used as digital signals for any circuits using gates, that you learnt in Unit 7 of this course. In Appendix-16A we have given the detailed data-sheet of IC555. You need not learn it by heart, but it will give you an idea, as to how the data-sheets of ICs look like and various parameters specified in it, which are useful for the designers of the circuits using that IC.

By proper choice of capacitor and resistor values we can design timer circuits having pulse width of as low as few microsecond or as large as few minutes. From the data sheet you will observe that the error in the timing is less than 2%. Hence the circuits built using IC555 give a very stable timing waveforms.

16.2.2 Block Diagram of IC555

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network.

You are already conversant with the voltage comparators, which are nothing but the operational amplifiers without any feedback. You may not have learnt about the flip-flop. But it is sufficient here to know that it is a digital circuit which has two inputs named set (*S*) and reset (*R*). The two outputs of the flip-flop are complementary to each other, that is, if one output is 1 then the second one is 0, and vice versa. The symbol of a flip-flop is shown in Fig. 16.2. The output of the flip-flop (*Q*) is set to high (1) when the set input (*S*) is high (1) and the output is low when the reset input (*R*) is high (1).

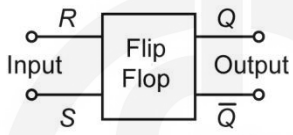


Fig. 16.2: **Symbol of flip-flop.**

In Fig. 16.3 we have shown a functional block diagram of IC555.

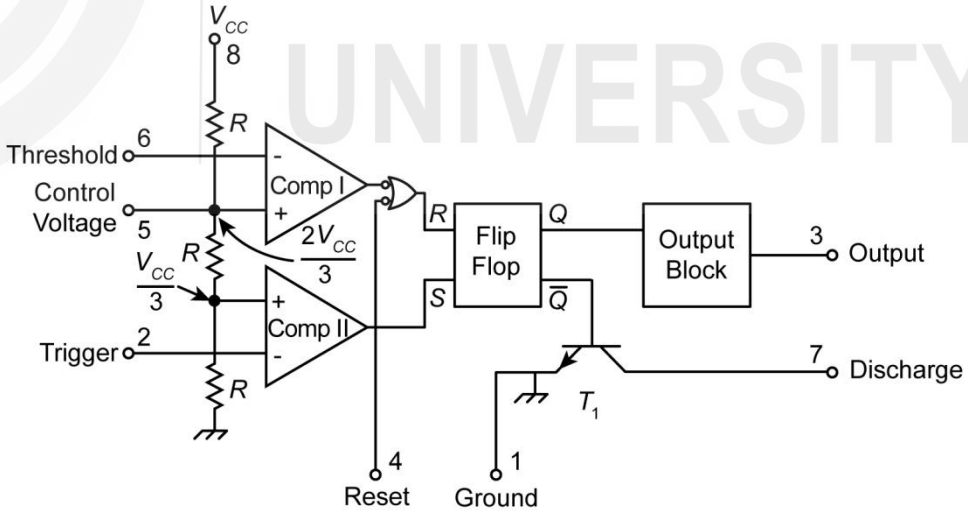


Fig. 16.3: **Functional block diagram of IC555.**

The value of each resistor in the voltage divider chain is 5 kΩ and there are three such resistors. In some reference it is stated that this fact gives rise to the designation **555** to this IC.

There are two comparators: Comparator I and Comparator II. There is a voltage divider in the form of a chain of three equal internal resistors of 5 kΩ each, connected between the inputs of the two comparators as shown in the figure.

This resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator (Comp-I) is

referenced internally at 2/3 of supply voltage level and the trigger comparator (Comp-II) is referenced at 1/3 of supply voltage. The outputs of Comp-I and Comp-II are tied to a flip-flop. The output *Q* of the flip-flop is used as the output of the IC (pin 3) while $\overline{Q}$, is connected to the base of the discharge transistor T_1, which operates in its non-linear mode (i.e. it is either cut-off or saturated). With base at low voltage ($\overline{Q}$ = 0), it is cut off while with $\overline{Q}$ = 1, it is fully *ON*.

When the trigger voltage is moved below 1/3 of the supply, the trigger comparator changes state and sets the flop-flop driving the output to a high state. Simultaneously, the transistor T_1 is switched *OFF* and the external timing capacitor starts charging. The threshold pin normally monitors the capacitor voltage of the timing network made of external resistor-capacitor, as will be described in the next sections. When the capacitor voltage exceeds 2/3 of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor (T_1) switches *ON*, thereby discharging the external timing capacitor. Once the capacitor is discharged, the timing cycle is completed, and the timer will await for the next trigger pulse.

16.2.3 Pin Functions

After understanding the internal functional blocks of IC555, let us now once again recapitulate the functions of eight pins of the IC.

Pin 1 (Ground): The ground (or common) pin is the most-negative supply potential of the device, which is normally connected to circuit common (ground) when operated from positive supply voltages.

Pin 2 (Trigger): This pin is the input to the trigger comparator (Comp-II) and is used to set the flip-flop, which in turn causes the output to go high. This is the beginning of the timing sequence in monostable operation. Triggering is accomplished by taking the pin from above to below a voltage level of $V_{CC}/3$. The trigger pulse must be of shorter duration than the time interval determined by the external *R* and *C*. The minimum width of the triggering pulse should be greater than 1 μs.

Pin 3 (Output): The pulsed / rectangular wave output of IC555 is obtained from this pin. The output voltage available at this pin is approximately equal to the V_{CC} applied to pin 8.

Pin 4 (Reset): This pin is used to externally reset the flip-flop and return the output to a low state. The reset input is an overriding function; that is, it will force the output of flip-flop to a low state regardless of the state of either of the other inputs. It may thus be used to terminate an output pulse prematurely. The pin is activated when a voltage level anywhere between 0 and 0.4 V is applied to the pin. When not used, it is recommended that the reset input be tied to V_{CC} to avoid any possibility of false resetting.

Pin 5 (Control Voltage): This pin allows direct access to the $2V_{CC}/3$ voltage-divider point i.e. the reference level for the threshold comparator (Comp-I). By applying a voltage to this pin, it is possible to vary the timing of the device independently of the external timing *RC* network. When not in use,

control-voltage pin is bypassed to ground, with a capacitor of about 0.01 μF (10 nF) for immunity to noise.

Pin 6 (Threshold): Pin 6 is one input to the upper comparator (the other being pin 5) and is used to reset the flip-flop, which causes the output to go low. Resetting via this terminal is accomplished by taking the terminal from below to above a voltage level of $2V_{CC}/3$.

Pin 7 (Discharge): This pin is connected to the open collector of discharge transistor T_1, the emitter of which is internally connected to ground. So that when the transistor is turned *ON*, pin 7 is effectively shorted to ground. Usually the timing capacitor is connected between pin 7 and ground and is discharged when the transistor turns *ON*. The conduction state of this transistor is identical in timing to that of the output stage. It is *ON* (low resistance to ground) when the output is low and *OFF* (high resistance to ground) when the output is high.

Pin 8 (V +): The V+ pin (also referred to as V_{CC}) is the positive supply voltage terminal of the 555 timer IC. Supply voltage operating range for IC 555 is between +5 volts and + 15 volts.

Before proceeding further to discuss the applications of IC555 timer, you may like to attempt an SAQ.

SAQ 1 – Trigger pulse to IC555

What should be the amplitude of negative going trigger pulse applied to pin 2 of IC555? Why?

The 555 timer is mainly used in two basic operation modes:

- Monostable (one-shot), Multivibrator; and
- Astable (oscillatory, free run mode) multivibrator.

Now we will discuss these modes of operation.

16.3 MONOSTABLE MULTIVIBRATOR USING IC555

This configuration requires only two external components for operation as can be seen from Fig. 16.4.

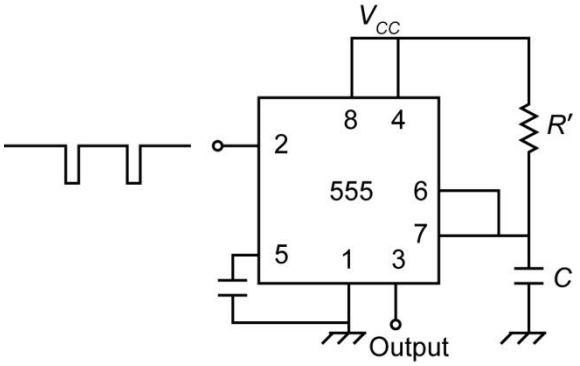


Fig. 16.4: **Monostable multivibrator.**

The sequence of events starts when a voltage below $V_{CC}/3$ is sensed by the trigger comparator (Comp-II). The trigger is normally applied in the form of a short negative-going pulse. On the negative-going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns *OFF*. Note that prior to the input trigger pulse, the discharge transistor is *ON*, shorting the timing capacitor to the ground. After trigger action, the timing capacitor, *C* starts charging through the timing resistor, *R′*. The voltage on the capacitor increases exponentially with a time constant $T = R'C$. Ignoring capacitor leakage, the capacitor will reach the $2V_{CC}/3$ level in 1.1 time constants or

$$t_p = 1.1R'C \qquad (16.1)$$

where t_p is in seconds, *R′* is in ohms, and *C* is in farads. This voltage level changes the output state of the threshold comparator (Comp-I), which in turn drives the output of the flip-flop low and turns the discharge transistor *ON*. The transistor discharges the capacitor *C* rapidly. The timer has completed its cycle and will now await another trigger pulse.

Fig. 16.5 shows the waveforms of the monostable operation. The top most waveform is the trigger pulse input given to pin 2. Once the trigger pulse is applied Comp-II sets the flip-flop output (pin 3) to high state. Its voltage goes from 0 to V_{CC} volts. Simultaneously the discharge transistor T_1 switches *OFF* and the capacitor starts charging with *R′C* time constant. Initially the capacitor is fully discharged; hence it begins to charge from 0 V. It keeps on charging till the threshold comparator (Comp-I) changes its state. This happens when the capacitor voltage is $2V_{CC}/3$. At this moment the flip-flop is reset, output (pin 3) is at 0 V and transistor T_1 turns *ON*. This causes instant discharging of the capacitor to 0V.

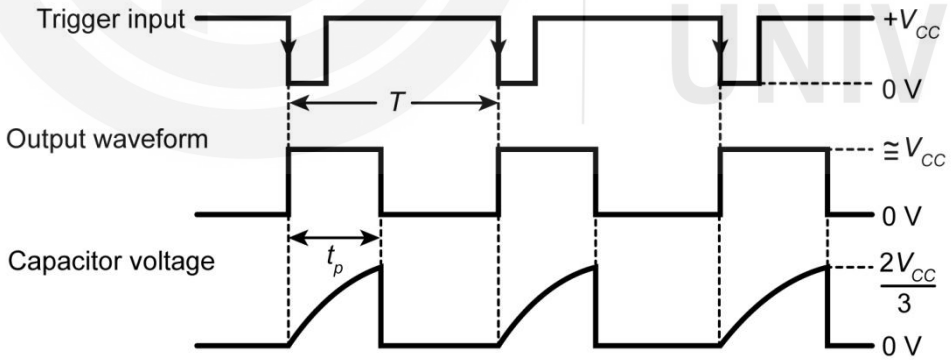


Fig. 16.5: **Waveforms of a monostable multivibrator.**

In this way we generate a pulse of width t_p at the output of the IC. This pulse width is determined by the relation given by Eq. (16.1).

To understand the function of a monostable multivibrator solve an SAQ.

SAQ 2 – Monostable multivibrator

Design a monostable multivibrator using IC555 to give a 100 ms long duration pulse when trigger input is applied.

After understanding the working of a monostable multivibrator, let us discuss another application of IC555 as an astable multivibrator.

16.4 ASTABLE MULTIVIBRATOR USING IC555

In the monostable multivibrator we obtain a single pulse at the output of the multivibrator circuit in response to a trigger pulse. But if we require to generate a continuous rectangular wave at the output of the multivibrator, we need to automatically generate a trigger within the circuit. This principle is used in the design of a free running rectangular wave oscillator or an astable multivibrator. Such continuous waveform generator has many applications like a square wave oscillator providing reference clock pulses to some digital circuit or a free running ramp generator, which uses the waveforms across the timing capacitor.

The circuit diagram of an astable multivibrator using IC555 is shown in Fig. 16.6.

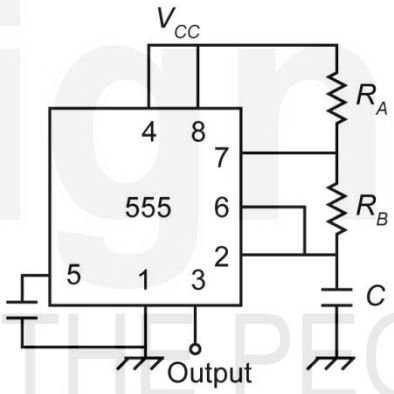


Fig. 16.6: **Astable multivibrator.**

In the astable (free-run) mode, only one additional component, R_B, is necessary. The trigger is now tied to the threshold pin. At the time when power is switched on, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charging path through R_A and R_B. When the capacitor reaches the threshold level of $2V_{CC}/3$ the output drops low and the discharge transistor turns *ON*.

The timing capacitor now discharges through R_B. When the capacitor voltage drops to $V_{CC}/3$, the trigger comparator changes its state, automatically re-triggering the timer, creating a continuously running oscillator circuit.

The waveforms generated by the astable multivibrator at the output pin 3 and across the capacitor (between pin 6 and ground) are shown in Fig. 16.7. (Here we have omitted the first wave cycle just after power on, when capacitor charges from 0 V to $2V_{CC}/3$ V.)

The upper waveform represents the rectangular wave output. You must have noticed that the *ON* time of this rectangular waveform is decided by the charging time of the capacitor while the *OFF* time is determined by the discharging time of the capacitor.

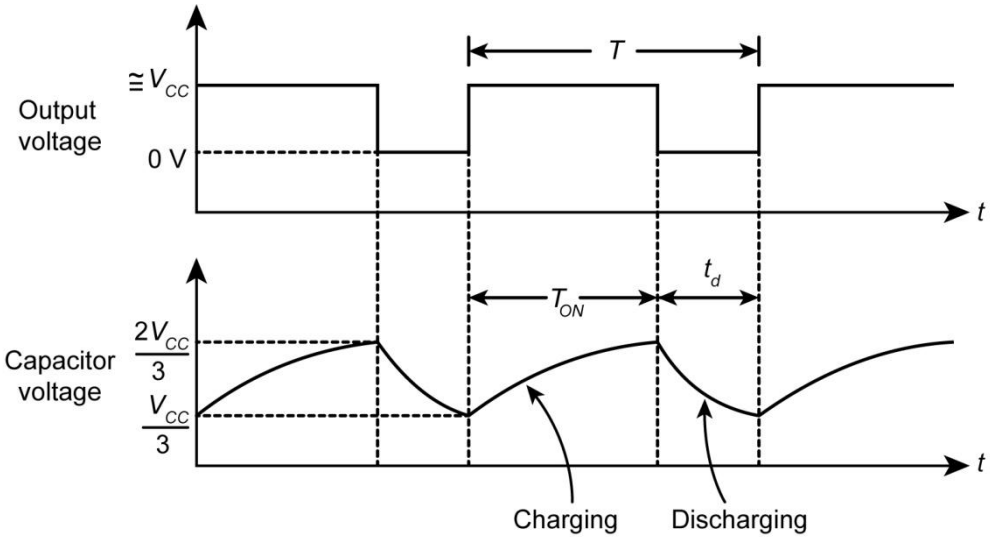


Fig. 16.7: **Waveforms of an astable multivibrator.**

So the *ON*-time (high) of output is the time taken by the capacitor to charge from $V_{CC}/3$ to $2V_{CC}/3$ through resistors R_A and R_B.

$$\therefore \quad T_{ON} = 0.69(R_A + R_B)C \qquad (16.3)$$

where R_A and R_B are in ohms and *C* is in farads.

Similarly, the *OFF*-time of the waveform is the time taken by the capacitor to discharge from $2V_{CC}/3$ to $V_{CC}/3$ through resistor R_B.

$$\therefore \quad T_{OFF} = 0.69 R_B C \qquad (16.4)$$

where R_B is in ohms and *C* is in farads.

Hence the total period of one cycle of the output waveform

$$\begin{aligned} T_{TOTAL} &= T_{ON} + T_{OFF} \\ &= 0.69(R_A + R_B)C + 0.69 R_B C \\ &= 0.69(R_A + 2R_B)C \end{aligned} \qquad (16.5)$$

The frequency of this rectangular wave oscillator is

$$\begin{aligned} f &= \frac{1}{T_{TOTAL}} = \frac{1}{0.69(R_A + 2R_B)C} \\ &= \frac{1.45}{(R_A + 2R_B)C} \end{aligned} \qquad (16.6)$$

Now, when we characterize a rectangular waveform, alongwith its frequency, we also specify its **duty cycle**. Duty cycle of a waveform is defined as

$$\text{Duty Cycle} = DC = \frac{T_{ON}}{T_{TOTAL}} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \qquad (16.7)$$

Sometimes it is also expressed in percentage as

$$\%\text{Duty Cycle} = \frac{T_{ON}}{T_{TOTAL}} \times 100\% \qquad (16.7a)$$

Substituting the values of T_{ON} and T_{TOTAL} from Eqs. (16.3) and (16.5) we get

$$\begin{aligned} \text{Duty Cycle} &= \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C} \\ &= \frac{R_A + R_B}{R_A + 2R_B} \end{aligned} \qquad (16.8)$$

A special case of rectangular waveform is a square waveform, when $T_{ON} = T_{OFF}$ or the duty cycle = 50%.

You will notice that an almost square waveform (duty cycle = 0.5 or 50%) is available by making R_B much larger than R_A. However, if we wishes to have the duty cycle less than 0.5, say 0.1 (= 1/10), then a strange situation arises. In such case R_A must be negative, which is absurd. So the conventional circuit is incapable of producing duty cycles of 0 – 50%.

In order to obtain a train of pulses for which the duty cycle should be less than 50%, one or two diodes that separate the charging path from the discharging path for the timing capacitor *C* might be used. One such circuit is shown in Fig. 16.8.

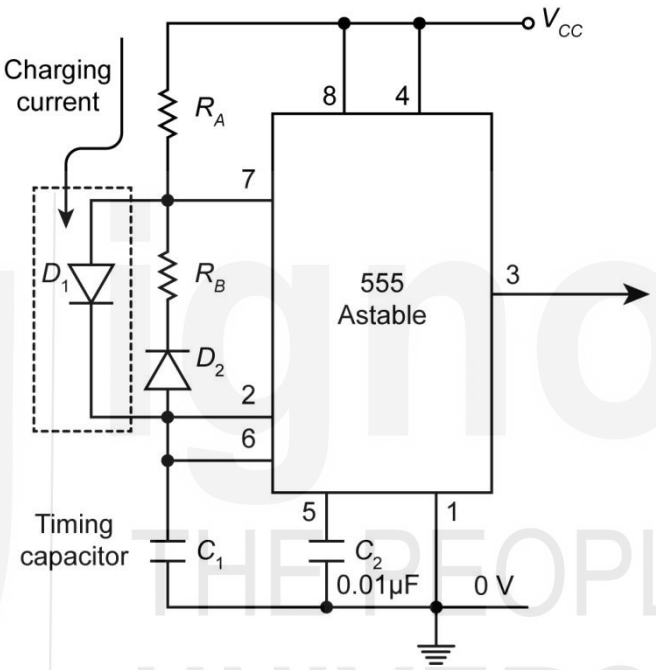


Fig. 16.8: **Astable multivibrator circuit to produce duty cycles of less than 50%.**

In circuit of Fig. 16.8, the capacitor charges through resistor R_A and diode D_1 whereas the capacitor discharges through the series combination of resistor R_B and diode D_2. Neglecting the forward resistance of the diodes we can write

$$T_{ON} = 0.69 R_A C$$

and

$$T_{OFF} = 0.69 R_B C$$

$$\therefore \quad T_{TOTAL} = 0.69 (R_A + R_B) C \qquad (16.9)$$

and

$$\text{Duty Cycle} = \frac{R_A}{R_A + R_B} \qquad (16.10)$$

Now with $R_A = R_B$, we can get a square wave (50% duty cycle) and when R_A is smaller than R_B, we can have duty cycle less than 50%.

In this case the frequency of oscillations is given by

$$f = \frac{1}{T_{TOTAL}} = \frac{1.45}{(R_A + R_B) C} \qquad (16.11)$$

SAQ 3 – Astable multivibrator with large duty cycle

Design an astable multivibrator with 1 kHz frequency and 60% duty cycle.

You have learnt about the IC555 and its applications in this unit. You will use them in your laboratory course allied with this theory course (BPHEL-144).

Let us now summarise the points covered in this unit.

16.5 SUMMARY

Concept	Description
IC555	■ It is an 8 pin timer IC useful for building multivibrator circuits. It can be operated in monostable (mono-shot) mode or astable (free running) mode.
Functional blocks of IC555	■ Two comparators, one flip-flop and a discharging transistor are the main blocks. The reference voltages of comparators are derived from an internal chain of three resistors of 5 kΩ each.
Monostable multivibrator	■ It requires one external resistor and a charging capacitor. The pulse width obtained after applying trigger input is given by $t_p = 1.1CR'$
Astable multivibrator	■ It requires two external resistors and a charging capacitor. The frequency is given by $f = \frac{1.45}{(R_A + 2R_B)C}$ and the duty cycle by $\text{DC} = \frac{R_A + R_B}{R_A + 2R_B}$ To obtain 50% or lower duty cycle special circuit with diodes is required.

16.6 TERMINAL QUESTIONS

1. What will be the effect on the frequency of an astable multivibrator if the supply voltage to IC555 is increased from 5 V to 10 V?
2. Why is it necessary to have a very narrow triggering pulse to a monostable multivibrator?
3. Design and draw the circuit of an astable multivibrator to given 10 kHz frequency pulse waveform with 50% duty cycle.
4. In a monostable multivibrator the pulse width t_p is 100 ms. What will be the effect on the output if another narrow trigger pulse arrives at 80 ms interval?

16.7 SOLTUIONS AND ANSWERS

Self-Assessment Questions

1. It should be lesser than $V_{CC}/3$. The reason is, the trigger pulse is applied to the trigger comparator (Comp-II). The non-inverting terminal of this comparator is kept at $V_{CC}/3$ due to the last resistor in the voltage divider

chain. If this comparator has to change its output state (from 0 to 1), the voltage at inverting input (trigger) should be lower than $V_{CC}/3$.

2. We need a pulse with $t_p = 100\,\text{ms}$. From Eq. (16.1) we have

$$t_p = 1.1R'C$$

Let us choose $C = 1\mu\text{F} = 1\times10^{-6}\text{F}$.

$$t_p = 100\,\text{ms} = 100\times10^{-3}\text{s} = 0.1\text{s}$$

$$\therefore \quad R' = \frac{t_p}{1.1C} = \frac{0.1}{1.1\times1\times10^{-6}}$$

$$= 0.091\times10^{6}\Omega = .91\text{k}\Omega$$

3. Since duty cycle is 60%, we use the circuit shown in Fig. 16.6.

Frequency = 1 kHz

$$\therefore \quad \text{Period} = \frac{1}{f} = 1\text{ms} = 1\times10^{-3}\text{s}$$

From Eq. (16.5),

$$T_{TOTAL} = 0.69(R_A + 2R_B)C$$

If we choose, $C = 10\,\text{nF} = 10\times10^{-9}\text{F}$, then

$$R_A + 2R_B = \frac{T_{TOTAL}}{0.69C} = \frac{1.45\,T_{TOTAL}}{C}$$

$$= \frac{1.45\times1\times10^{-3}\text{s}}{10\times10^{-9}\,\text{F}}$$

$$= 145\,\text{k}\Omega$$

The Duty cycle = 60% = 0.6.

From Eq. (16.8)

$$\frac{R_A + R_B}{R_A + 2R_B} = 0.6$$

$$\therefore \quad R_A + R_B = 0.6(R_A + 2R_B)$$

$$= 0.6\times145\,\text{k}\Omega = 87\,\text{k}\Omega$$

Now, $R_B = (R_A + 2R_B) - (R_A + R_B)$

$$= 145\,\text{k}\Omega - 87\,\text{k}\Omega$$

$$= 58\,\text{k}\Omega$$

$$\therefore \quad R_A = 87\,\text{k}\Omega - 58\,\text{k}\Omega = 29\,\text{k}\Omega$$

Hence the astable multivibrator with

$$R_A = 29\,\text{k}\Omega,\ R_B = 58\,\text{k}\Omega \quad \text{and} \quad C = 10\,\text{nF}$$

will provide 1 kHz wave with 60% duty cycle.

Terminal Questions

1. The frequency of the atable multivibrator is given by

$$f = \frac{1.45}{(R_A + 2R_B)C}$$

It indicates that it is independent of the supply voltage. For any value of supply voltage, the frequency would remain the same.

2. In a monostable multivibrator, once the trigger pulse is given, the output goes high for a pre-decided time period, t_p . The low going trigger initiates this pulse output by setting the flip-flop output to high and switching *OFF* the discharging transistor. This causes the capacitor to charge. When the capacitor voltage crosses $2V_{CC}/3$, the flip-flop should be reset and capacitor should discharge. But if the width of the trigger pulse is larger than period t_p , then, the trigger comparator output still keeps the flip-flop output in high state and capacitor discharge does not begin. This elongates the output pulse beyond t_p period.

3. For 50% duty cycle, we use the circuit shown in Fig. 16.8. If we neglect the diode forward resistance, the period of the waveform is given by Eq. (16.9)

$$T_{TOTAL} = 0.69(R_A + R_B)C$$

and duty cycle by Eq. (16.10).

$$\text{Duty cycle} = \frac{R_A}{R_A + R_B}$$

For 10 kHz frequency

$$T_{TOTAL} = \frac{1}{f} = 10^{-4}\,\text{s}$$

If we take C = 1 nF,

$$T_{TOTAL} = 0.69(R_A + R_B) \times 1 \times 10^{-9}\,\text{F} = 10^{-4}\,\text{s}$$

$$\therefore \quad R_A + R_B = 1.45 \times 1 \times 10^5\,\Omega = 145\,\text{k}\Omega$$

For 50% duty cycle,

$$R_A = R_B$$

$$\therefore \quad R_A + R_B = \frac{145 \times 10^3}{2} = 72.5\,\text{k}\Omega$$

4. If the monostable multivibrator output is set to high value by a trigger pulse, it continues to remain high till the capacitor charges up to $2V_{CC}/3$ voltage. In the meantime, even if another trigger pulse comes, the capacitor charging process is not affected and the second trigger arriving before 100 ms period is over, is ignored and there is no effect on the output of the monostable multivibrator.

APPENDIX-16A: DATA-SHEET OF IC555

Electrical Characteristics $T_A = 25°C, V_{CC} = +5V$ to $+15$ unless otherwise specified.

Parameter	Test Conditions	SE 555			Units
		Min.	Typical	Max.	
Supply voltage		4.5		16	V
Supply current	$V_{CC} = 5\,V\, R_L = \infty$		3	6	mA
	$V_{CC} = 15\,V\, R_L = \infty$		10	15	mA
Timing Error					
Initial Accuracy	$R_A = 1k\Omega$ to $100k\Omega$		1		%
Drift with Temperature	C = 0.1 μF		50		ppm / °C
Drift with Supply Voltage			0.1		% / Volt
Threshold Voltage			2/3		X V_{CC}
Trigger Voltage	$V_{CC} = 15\,V$		5		V
	$V_{CC} = 5\,V$		1.67		V
Trigger Current			0.5	0.9	μA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current			0.1	0.25	μA
Control Voltage Level	$V_{CC} = 15\,V$	9	10	11	V
	$V_{CC} = 5\,V$	2.6	3.33	4	V
Output Voltage Drop (low)	$V_{CC} = 15\,V$				
	$I_{SINK} = 10\,mA$		0.1	0.25	V
	$I_{SINK} = 50\,mA$		0.4	0.75	V
	$I_{SINK} = 100\,mA$		2.0	2.5	V
	$I_{SINK} = 200\,mA$		2.5		V
	$V_{CC} = 5\,V$				
	$I_{SINK} = 5\,mA$		0.25	0.35	V
Output Voltage Drop (high)	$I_{SOURCE} = 200\,mA$				
	$V_{CC} = 15\,V$		12.5		V
	$I_{SOURCE} = 100\,mA$				
	$V_{CC} = 15\,V$	12.75	13.3		V
	$V_{CC} = 5\,V$	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Ref.: From the Texas Instruments website: www.ti.com

FURTHER READINGS

1. **Electronic Principles** by Malvino A.P., Tata McGraw Hill Publishing Co. Ltd., 3rd Edition, Fifteenth Reprint (1992).

2. **Integrated Electronics: Analog and Digital Circuits and Systems** by Millman, J. and Halkias, C.C., McGraw Hill Book Co., International Edition, 29th Printing (1986).

3. **Op Amps and Linear Integrated Circuits** by Gayakwad, R.A., Prentice-Hall of India, 4th Edition, 26th Printing (2002).

4. **Operational Amplifiers** by Clayton, G.B., Winder, S., Elsevier, 5th Edition (2008).

TABLE OF PHYSICAL CONSTANTS

Symbol	Quantity	Value
c	Speed of light in vacuum	3.00×10^{8} ms^{-1}
μ_0	Permeability of free space	1.26×10^{-6} NA^{-2}
ε_0	Permittivity of free space	8.85×10^{-12} C^2 N^{-1}m^{-2}
$1/4\pi\varepsilon_0$		8.99×10^{9} Nm^2 C^{-2}
e	Charge of the proton	1.60×10^{-19} C
$-e$	Charge of the electron	-1.60×10^{-19} C
h	Planck's constant	6.63×10^{-34} Js
$\hbar$	$h / 2\pi$	1.05×10^{-34} Js
m_e	Electron rest mass	9.11×10^{-31} kg
$-e/m_e$	Electron charge to mass ratio	-1.76×10^{11} Ckg^{-1}
m_p	Proton rest mass	1.67×10^{-27} kg (1 amu)
m_n	Neutron rest mass	1.68×10^{-27} kg
a_0	Bohr radius	5.29×10^{-11} m
N_A	Avogadro constant	6.02×10^{23} mol^{-1}
R	Universal gas constant	8.31 Jmol^{-1}K^{-1}
k_B	Boltzmann constant	1.38×10^{-23} J K^{-1}
G	Universal gravitational constant	6.67×10^{-11} Nm^2 kg^{-2}

LIST OF BLOCKS AND UNITS: BPHET-143

BLOCK 1: PHYSICS OF SEMICONDUTOR DIVICES

BLOCK 2: DIGITAL CIRCUITS

BLOCK 3: ANALOG CIRCUITS

BLOCK 4: OPERATIONAL AMPLIFIER AND INSTRUMENTATION

SYLLABUS: DIGITAL AND ANALOG CIRCUITS AND INSTRUMENTATION (BPHET-143) 4 Credits

Physics of Semiconductor Devices: Bonding in semiconductors, intrinsic and extrinsic semiconductors, concept of band gap and its consequences, concept of hole – drift and diffusion current, *I-V* characteristics of a semiconductor, gradient driven flow, parameters governing carrier mobility (drift velocity, saturation of drift velocity and breakdown). Formation of *p-n* junction, barrier potential, *I-V* characteristics of *p-n* junction diode, current flow mechanism under forward and reverse bias conditions (drift, diffusion and recombination), *p-n* junction diode as a rectifier, other types of diodes – Zener, LED, solar cell, photodetectors (construction, working and nature of *I-V* characteristics). Double junction devices (bipolar junction transistor and field effect transistor) – construction, working mechanisms, biasing conditions (for *n-p-n* and *p-n-p* transistors), CE, CB, CC configurations of BJT, transistor biasing methods, input-output characteristics of common emitter (CE) configuration – cut-off, active and saturation regions, current gains α and β and their relationship, load line and quiescent operating point (linear and switching operations of transistor). Equivalent circuit of transistor, *h*-parameter equivalent circuit, analysis of CE amplifier using hybrid model – input and output impedances, current, voltage and power gain.

Digital Circuits: Binary, octal, hex, decimal number systems and their interconversions, codes (BCD and ASCII), Boolean arithmetic, Boolean theorems, D'Morgan's theorem, logic gate (AND, OR, NOT, NAND, NOR, XOR, XNOR), symbols, truth tables, gate circuit realization using diodes and transistors. Simplification of logic circuits using Boolean algebra, fundamental products, minterms and maxterms, conversion of a truth table into an equivalent logic circuit by (1) sum of products (SOP) method and (2) Karnaugh map. Binary addition, binary subtraction (using 2's complement method), half adder, full adder and subtractor, 4-bit binary adder-subtractor.

Analog Circuits: Amplifiers: Classification of amplifiers (*A,B, AB, C*) with applications, small signal-low frequency amplifiers, power amplifiers – push-pull amplifier, negative feedback and its effect on amplifier performance, cascade amplifiers – coupling networks and gain calculation.

Oscillators: Positive feedback and oscillators, Barkhausen criterion for self-sustained oscillations, classification of oscillators RF – *L-C* oscillator (Colpitt's and Hartley oscillators, circuits, working and design), AF – *R-C* oscillator (Wein bridge and phase shift oscillators, frequency determination, circuits, working and design)

Power supplies: Rectifiers (HW, FW – bridge, centre tapped), calculation of ripple factor, rectification efficiency, filters (*R-C, L-C*), voltage regulation by potential divider, Zener diode and series pass voltage regulator.

Operational Amplifier and Instrumentation: Op-Amp: Virtual ground, ideal op-amp and IC-741 characteristics (transfer, offset, bandwidth, CMRR, slew rate), common and differential mode gains, op-amp as a comparator, zero crossing detector, feedback in op-amp, inverting and non-inverting amplifier, op-amp as an adder, subtractor, differentiator, integrator.

Instrumentation: Introduction to CRO, block diagram, functions and knobs on CRO panel, applications of CRO to study waveforms, measurement of voltage, frequency and phase, (mention of digital storage oscilloscope), timer IC 555, block diagram, pin-out diagram and its application as a stable and monostable multivibrator.